Gain and Attenuation Volume Controller IC 4 Sets of Stereo Input, Low voltage Gain and Attenuation 15~-79dB

FEATURES

- Operation range: 2.7V~6.5V.
- Low power consumption.
- Gain/Attenuation: 15dB to –79dB.
- +1dB/step, -1dB/step and -10dB/step are controlled independently.
- Good PSRR and low pop noise.
- I^2C interface.
- Housed in 16 pin SSOP package.

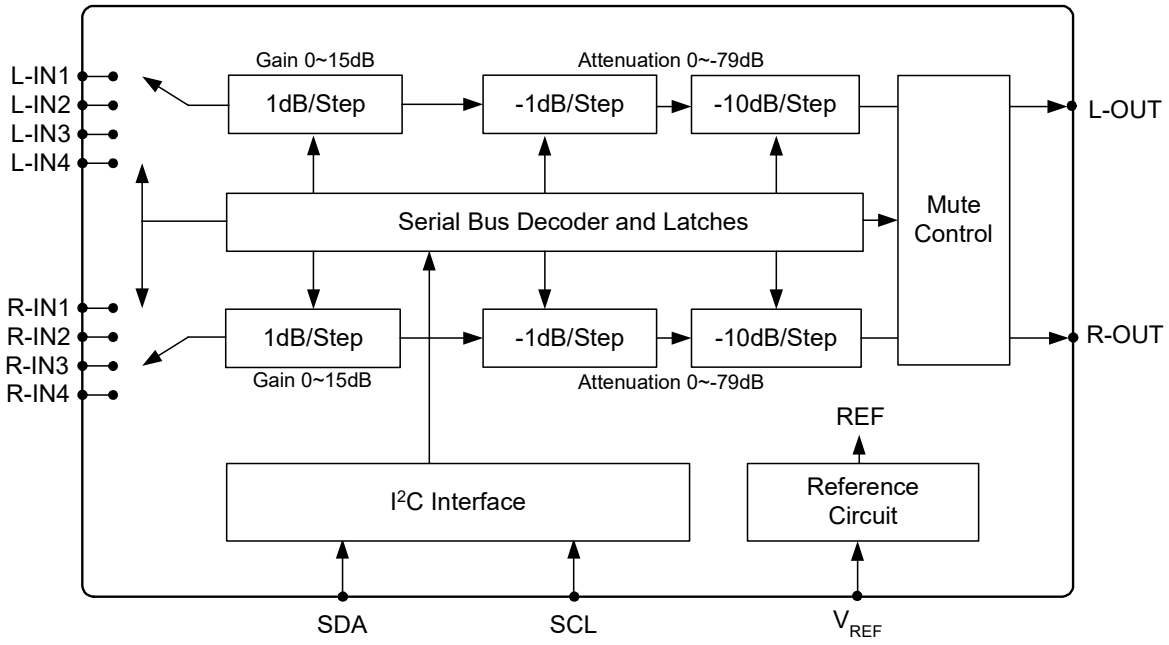
APPLICATIONS

- Multimedia system.
- Hi-Fi audio system.
- MP3，PDA.

DESCRIPTION

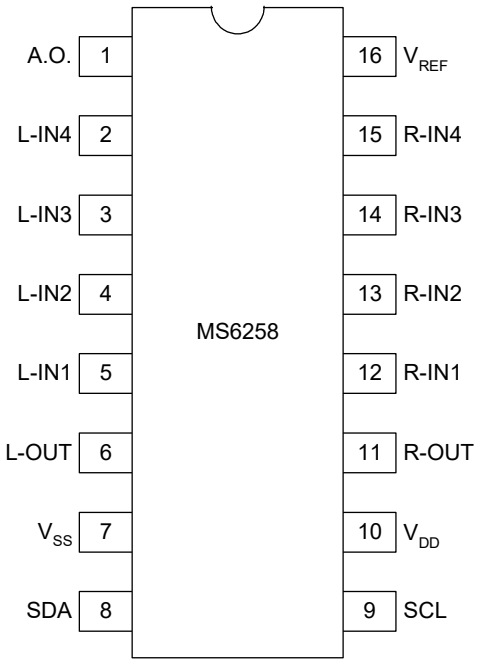
The MS6258 is a stereo audio volume controller IC with 4 sets of stereo input. It uses CMOS technology specially for the low voltage application with low noise, rail-to-rail output. The MS6258 provide an I^2C control interface with gain / attenuation range of 15dB to -79dB. The gain and attenuation, +1dB/step, -1dB/step and -10dB/step are controlled independently. The initial condition is set to be maximum attenuation –79dB (-70dB + -9dB), gain 0dB and mute on mode when the power is up.

BLOCK DIAGRAM



PIN CONFIGURATION

Symbol	Pin	Description
A.O.	1	Address option *
L-IN4	2	4th left channel input
L-IN3	3	3rdleft channel input
L-IN2	4	2nd left channel input
L-IN1	5	1st left channel input
L-OUT	6	Left channel output
V_{SS}	7	Ground
SDA	8	I^2C data input
SCL	9	I^2C clock input
V_{DD}	10	Positive supply voltage
R-OUT	11	Right channel output
R-IN1	12	1st right channel input
R-IN2	13	2nd right channel input
R-IN3	14	3rd right channel input
R-IN4	15	4th right channel input
V_{REF}	16	Reference voltage = $1/2V_{DD}$



Note: 1. Pin 1 is set to Lo or open , the address code is 88H (10001000B).
2. Pin 1 is set to Hi , the address code is 8CH (10001100B).
3. The V_{REF} connects a capacitor to Vss.

ORDERING INFORMATION

Package	Part number	Packaging Marking	Transport Media
16-Pin SSOP (lead free)	MS6258SSGTR	MS6258G	2.5k Units Tape and Reel
16-Pin SSOP (lead free)	MS6258SSGU	MS6258G	100 Units Tube

RoHS Compliance

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
VDD	Supply Voltage	6.5	V
V_{ESD}	Electrostatic Handling	-4500 to 4500	V
T_{STG}	Storage Temperature Range	-65 to 150	℃
T_A	Operating Ambient Temperature Range	-40 to 85	℃
T_J	Maximum Junction Temperature	150	℃
T_S	Soldering Temperature, 10 seconds	260	℃
R_{THJA}	Thermal Resistance from Junction to Ambient in Free Air SSOP16	210	℃/W

OPERATING RATINGS

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply Voltage	2.7	-	6.5	V

5V ELECTRICAL CHARACTERISTICS

(V_{DD}=5.0V, V_{SS}=0V, Attenuation=0dB, Gain=0dB, f=1kHz, V_O=0dBV, V_{REF} Cap=10uF; unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DC Characteristics						
I_Q	Quiescent current		-	3.8	4.2	mA
A_{GA}	Gain/Attenuation	Max gain	-	15	-	dB
		Max attenuation	-	-79	-	dB
A_{STEP}	Gain/Attenuation step		-	1	-	dB
E_{GA}	Gain/Attenuation step error		-	0.3	-	dB
CS	Channel separation		95	105	-	dB
PSRR	Power supply rejection ratio	Vripple = -20dBV, 100Hz	-	53	-	dB
MUTE	Mute Attenuation	Vin=0dBV	-	85	-	dB
Rin	Input Impedance		18	20	-	kΩ
Rout	Output Impedance		-	50	100	Ω
AC Characteristics						
Vo	Maximum output voltage swing	(THD+N)/S < 0.1%	-	4.8	-	Vpp
THD+N	Total harmonic distortion plus noise		-	-69	-64	dB
S/N	Signal-to-noise ratio	V_O=4.5Vpp	95	100	-	dB
Bus Characteristics						
V_{IH}	Bus high input level		-	-	$0.7V_{DD}$	V
V_{IL}	Bus low input level		$0.3V_{DD}$	-	-	V

3.3V ELECTRICAL CHARACTERISTICS

(V_{DD}=3.3V, V_{SS}=0V, Attenuation=0dB, Gain=0dB, f=1kHz, V_O=-3dBV, V_{REF} Cap=10uF; unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DC Characteristics						
I_Q	Quiescent current		-	3.7	4.1	mA
CS	Channel separation		90	100	-	dB
PSRR	Power supply rejection ratio	Vripple = -20dBV, 100Hz	-	52	-	dB
MUTE	Mute Attenuation	Vin=-3dBV	-	80	-	dB
AC Characteristics						
Vo	Maximum output voltage swing	(THD+N)/S < 0.1%	-	3	-	Vpp
THD+N	Total harmonic distortion plus noise		-	-69	-64	dB
S/N	Signal-to-noise ratio		85	90	-	dB

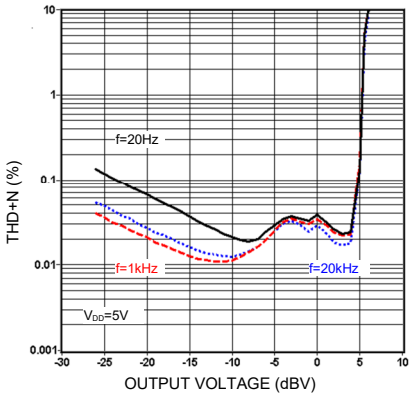
2.7V ELECTRICAL CHARACTERISTICS

(V_{DD}=2.7V, V_{SS}=0V, Attenuation=0dB, Gain=0dB, f=1kHz, V_O=-3dBV, V_{REF} Cap=10uF; unless otherwise specified)

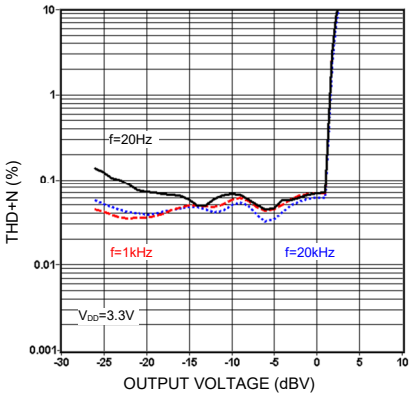
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DC Characteristics						
I_Q	Quiescent current		-	3.2	3.6	mA
CS	Channel separation		90	100	-	dB
PSRR	Power supply rejection ratio	Vripple = -20dBV, 100Hz	-	50	-	dB
MUTE	Mute Attenuation	Vin=-3dBV	-	80	-	dB
AC Characteristics						
Vo	Maximum output voltage swing	(THD+N)/S < 0.3%	-	2	-	Vpp
THD+N	Total harmonic distortion plus noise		-	-69	-64	dB
S/N	Signal-to-noise ratio		85	90	-	dB

TYPICAL PERFORMANCE CHARACTERISTICS

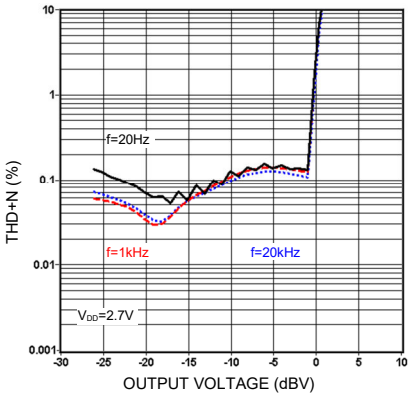
(Ta=25℃, V_{REF} Cap=10uF; unless otherwise specified)



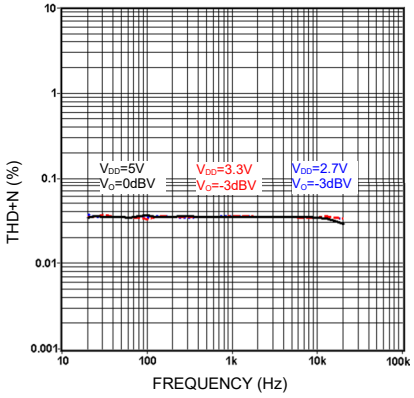
THD+N vs. output voltage



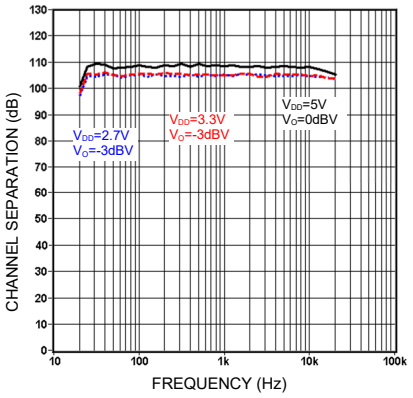
THD+N vs. output voltage



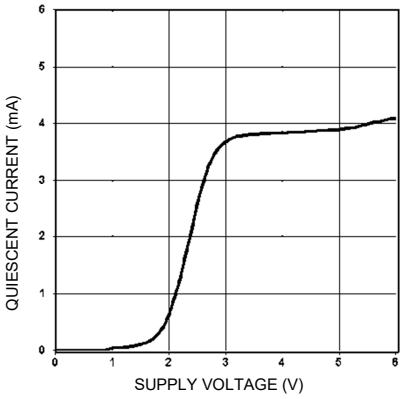
THD+N vs. output voltage



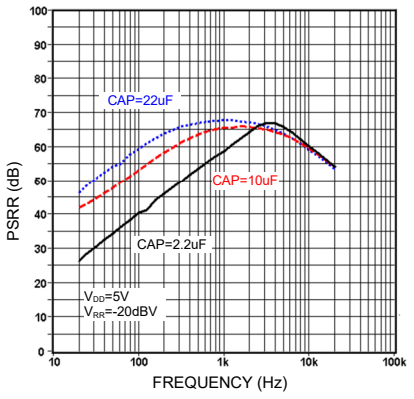
THD+N vs. frequency



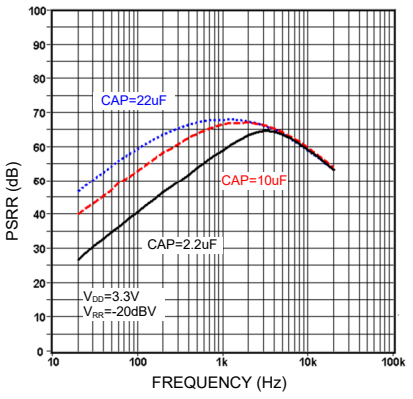
Channel separation vs. frequency



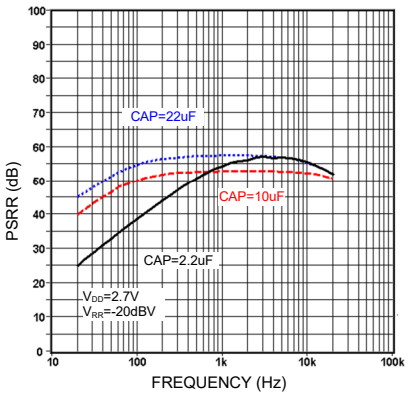
Quiescent current vs. supply voltage



PSRR vs. frequency



PSRR vs. frequency

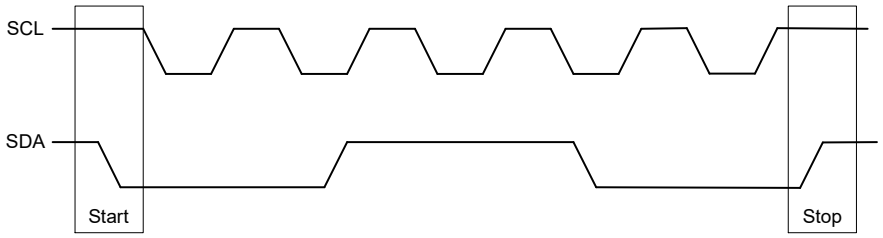


PSRR vs. frequency

I²C BUS DESCRIPTION

Start and stop conditions

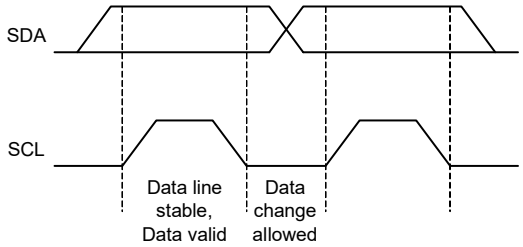
A start condition is activated when the SCL is set to HIGH and SDA shifts from HIGH to LOW state. The stop condition is activated when SCL is set to HIGH and SDA shifts from LOW to HIGH state. Please refer to the timing diagram below.



SCL : Serial Clock Line, SDA : Serial Data Line

Data validity

A data on the SDA line is considered valid and stable only when the SCL signal is in HIGH state. The HIGH and LOW states of the SDA line can only change when the SCL signal is LOW. Please refer to the figure below.

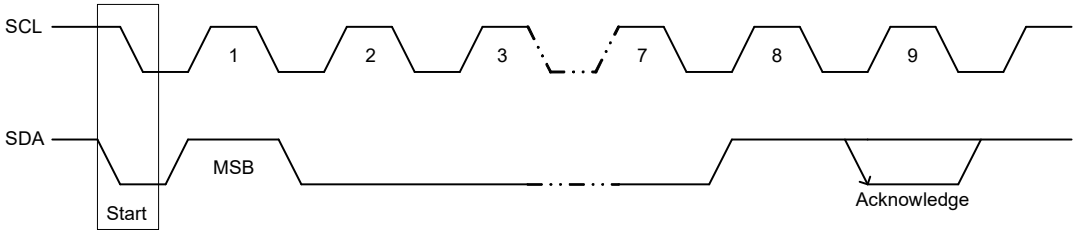


Byte format

Every byte transmitted to the SDA line consists of 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transmitted first.

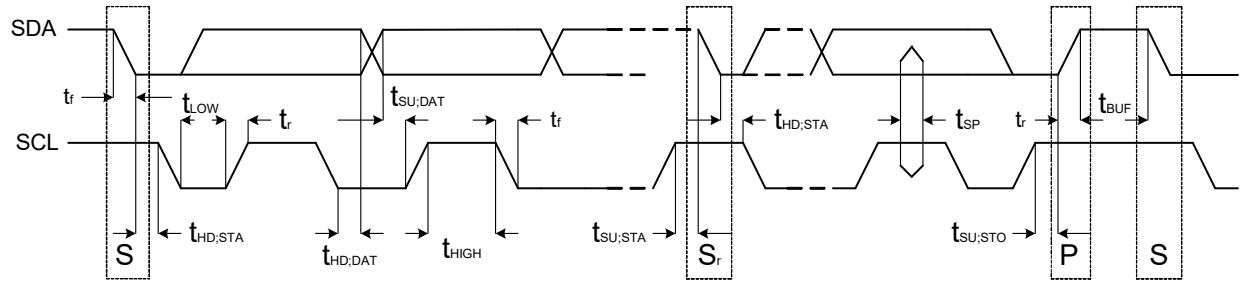
Acknowledge

During the Acknowledge clock pulse, the master (up) put a resistive HIGH level on the SDA line. The peripheral (audio processor) that acknowledges has to pull-down (LOW) the SDA line during the Acknowledge clock pulse so that the SDA line is in a stable LOW state during this clock pulse. Please refer to the diagram below.



The audio processor that has been addressed has to generate an Acknowledge after receiving each byte, otherwise, the SDA line will remain at the HIGH level during the ninth (9th) clock pulse. In this case, the master transmitter can generate the STOP information in order to abort the transfer.

Timing of SDA and SCL bus lines

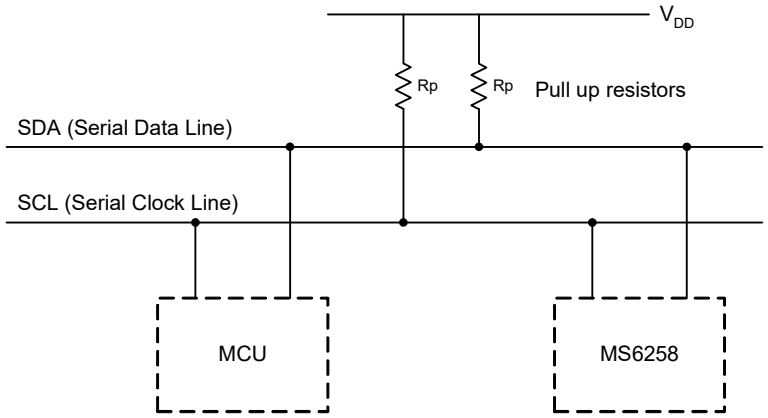


Standard mode

Symbol	Parameter	Min	Max	Unit
f_{SCL}	SCL clock frequency	0	100	kHz
$t_{HD:STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated	4.0	-	us
t_{LOW}	LOW period of the SCL clock	4.7	-	us
t_{HIGH}	HIGH period of the SCL clock	4.0	-	us
$t_{SU:STA}$	Set-up time for a repeated START condition	4.7	-	us
$t_{HD:DAT}$	Data hold time: For I^2C-bus devices	0	3.45	us
$t_{SU:DAT}$	Data-set-up time	250	-	ns
t_r	Rise time of both SDA and SCL signals	-	1000	ns
t_f	Fall time of both SDA and SCL signals	-	300	ns
$t_{SU:STO}$	Set-up time for STOP condition	4.0	-	us
t_{BUF}	Bus free time between a STOP and START condition	4.7	-	us
C_b	Capacitive load for each bus line	-	400	pF
V_{nL}	Noise margin at the LOW level for each connected device (including hysteresis)	$0.1V_{DD}$	-	V
V_{nH}	Noise margin at the HIGH level for each connected device (including hysteresis)	$0.2V_{DD}$	-	V

BUS INTERFACE

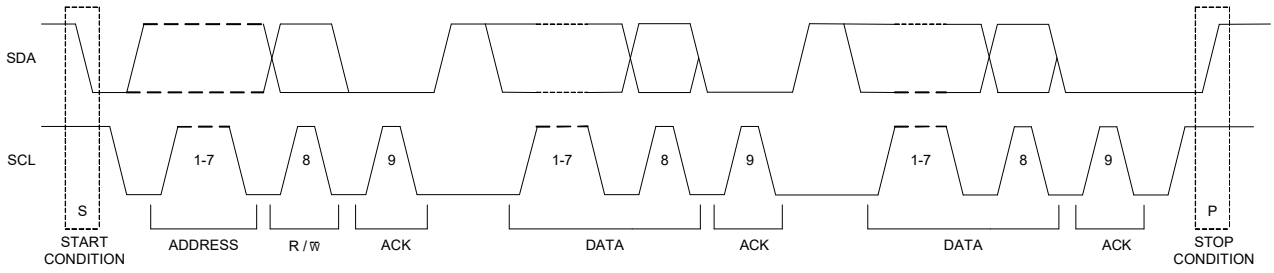
Data are transmitted to and from the MCU to the MS6258 via the SDA and SCL. The SDA and SCL make up the BUS interface. It should be noted that pull-up resistors must be connected to the positive supply voltage.



Interface protocol

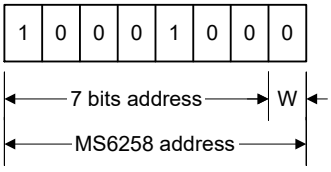
The format consists of the following

- A START condition
- A chip address byte including the MS6258 address. (7bits)
- The 8th bit of the byte must be "0".(write=0, read=1)
- MS6258 must always acknowledge the end of each transmitted byte.
- A data sequence (N-bytes + Acknowledge)
- A STOP condition

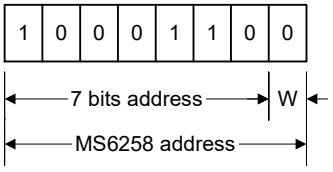


Protocol Address

Pin1(A.O.) = Low or Open



Pin1(A.O.) = High



Data bytes description

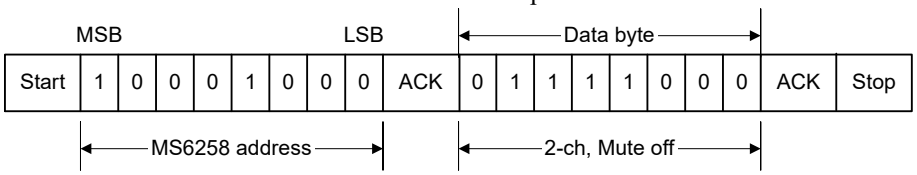
Function bits								
MSB							**LSB**	**Function**
1	1	1	1	1	1	1	1	Function off (-79dB)
1	1	0	1	A3	A2	A1	A0	2-channel, -1dB/step
1	1	1	0	0	B2	B1	B0	2-channel, -10dB/step
1	0	1	0	A3	A2	A1	A0	Left channel, -1dB/step
1	0	1	1	0	B2	B1	B0	Left channel, -10dB/step
0	0	1	0	A3	A2	A1	A0	Right channel, -1dB/step
0	0	1	1	0	B2	B1	B0	Right channel, -10dB/step
1	1	0	0	C3	C2	C1	C0	2-channel, +1dB/step
0	1	1	0	C3	C2	C1	C0	Left channel, +1dB/step
0	1	0	1	C3	C2	C1	C0	Right channel, +1dB/step
0	1	0	0	0	0	0	0	Stereo1
				0	0	0	1	Stereo2
				0	0	1	0	Stereo3
				0	0	1	1	Stereo4
0	1	1	1	0	0	0	1	Power off preparation (pop noise free)
				1	0	0	1	2-channel, mute On
				1	0	0	0	2-channel, mute Off

Gain / Attenuation bits						
A3	**A2**	**A1**	**A0**	**Attenuation (dB)**		**Gain (dB)**
-	**B2**	**B1**	**B0**	**A**	**B**	**C**
C3	**C2**	**C1**	**C0**			
0	0	0	0	0	0	0
0	0	0	1	-1	-10	+1
0	0	1	0	-2	-20	+2
0	0	1	1	-3	-30	+3
0	1	0	0	-4	-40	+4
0	1	0	1	-5	-50	+5
0	1	1	0	-6	-60	+6
0	1	1	1	-7	-70	+7
1	0	0	0	-8	-	+8
1	0	0	1	-9	-	+9
1	0	1	0	-	-	+10
1	0	1	1	-	-	+11
1	1	0	0	-	-	+12
1	1	0	1	-	-	+13
1	1	1	0	-	-	+14
1	1	1	1	-	-	+15

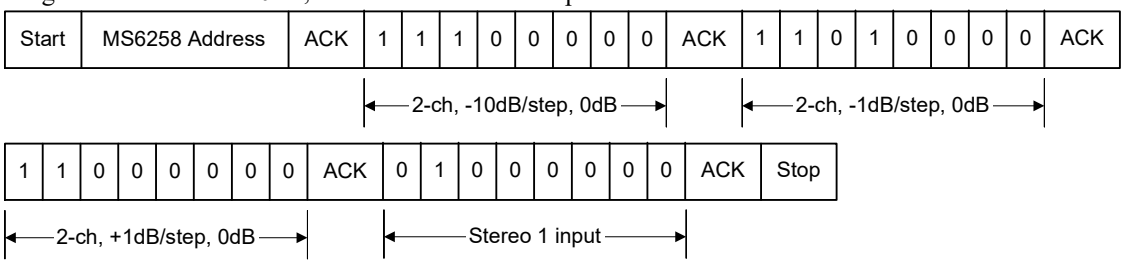
1. Attenuation bit, Ax = -1dB/step, Bx = -10dB/step
2. Gain bit, Cx = +1dB/step
3. Total gain / attenuation equal Ax + Bx + Cx.
4. The function of power off preparation is to prevent pop noise when power off.

Example

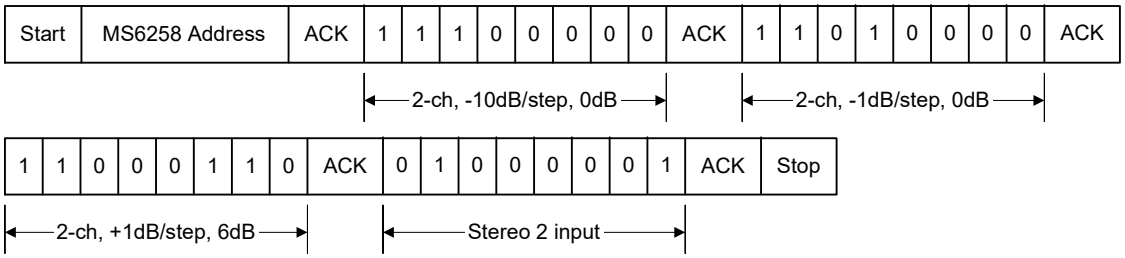
Mute off
The initial condition is –79dB and mute on when power on. The first command must disable the mute function.



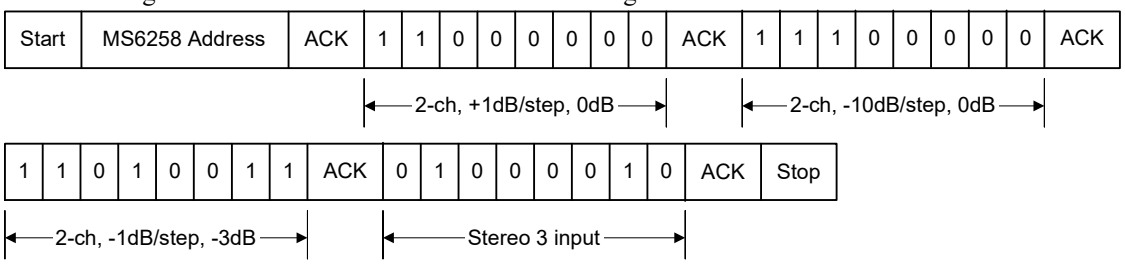
Set gain of 2 channel at 0dB, and selected stereo 1 input.



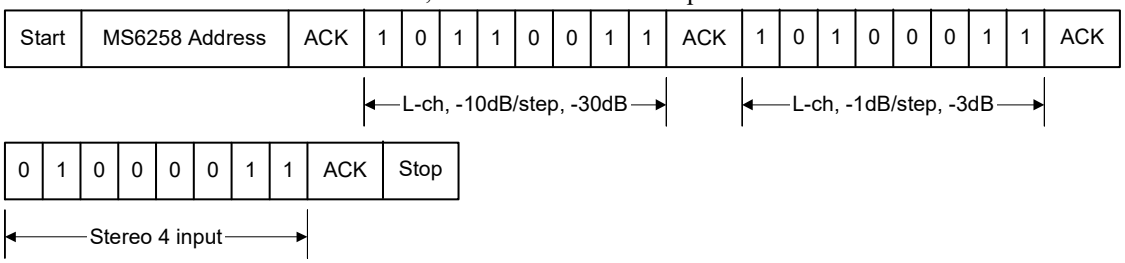
Set gain of 2 channel at 6dB, and selected stereo 2 input.
The value of attenuation must be set zero when the volume from attenuation to gain.



Set gain of 2 channel at -3dB, and selected stereo 3 input.
The value of gain must be set zero when the volume from gain to attenuation.

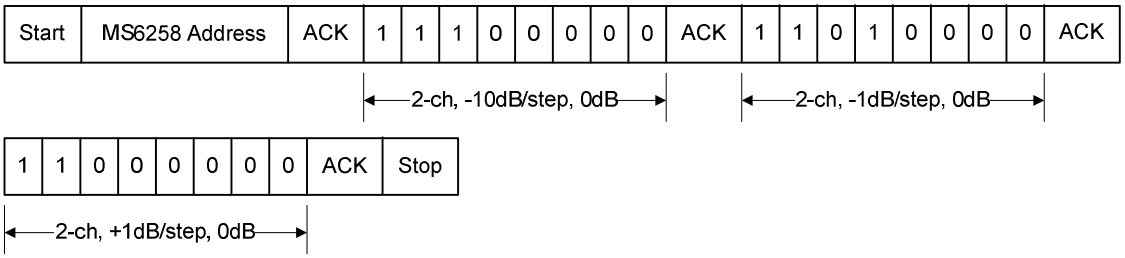


Set attenuation of left channel at –33dB, and selected stereo 4 input.

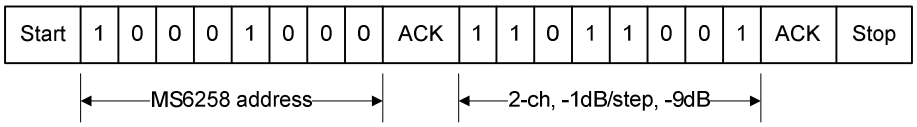


An example of the volume control. (Volume = Ax + Bx + Cx)

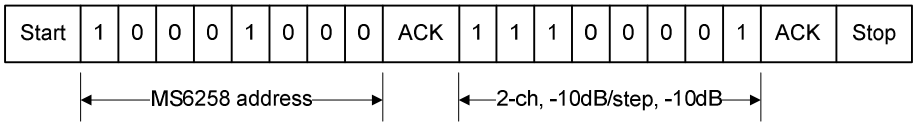
Set two channels at 0dB. (Ax + Bx + Cx = 0dB + 0dB + 0dB)



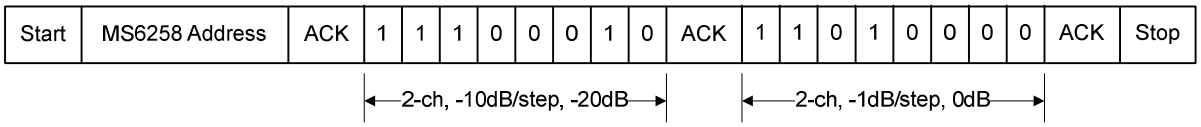
next, the volume changes from 0dB to -9dB. (Ax + Bx + Cx = -9dB + 0dB + 0dB)



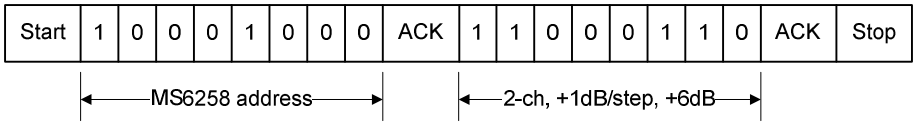
next, the volume changes from -9dB to -19dB. (Ax + Bx + Cx = -9dB + -10dB + 0dB)



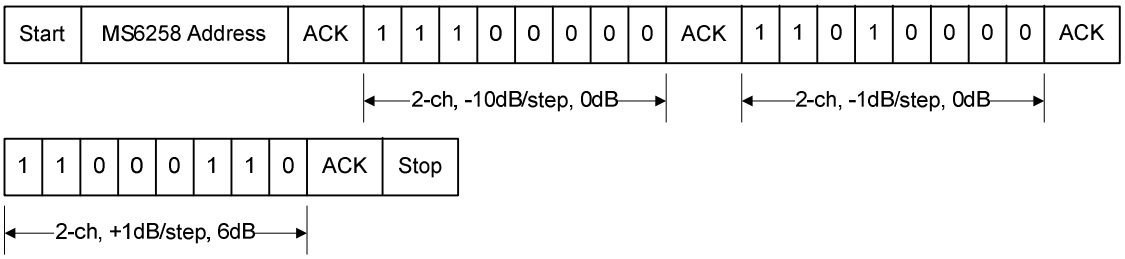
next, the volume changes from -19dB to -20dB. (Ax + Bx + Cx = 0dB + -20dB + 0dB)



next, the volume changes from -20dB to -14dB. (Ax + Bx + Cx = 0dB + -20dB + 6dB)



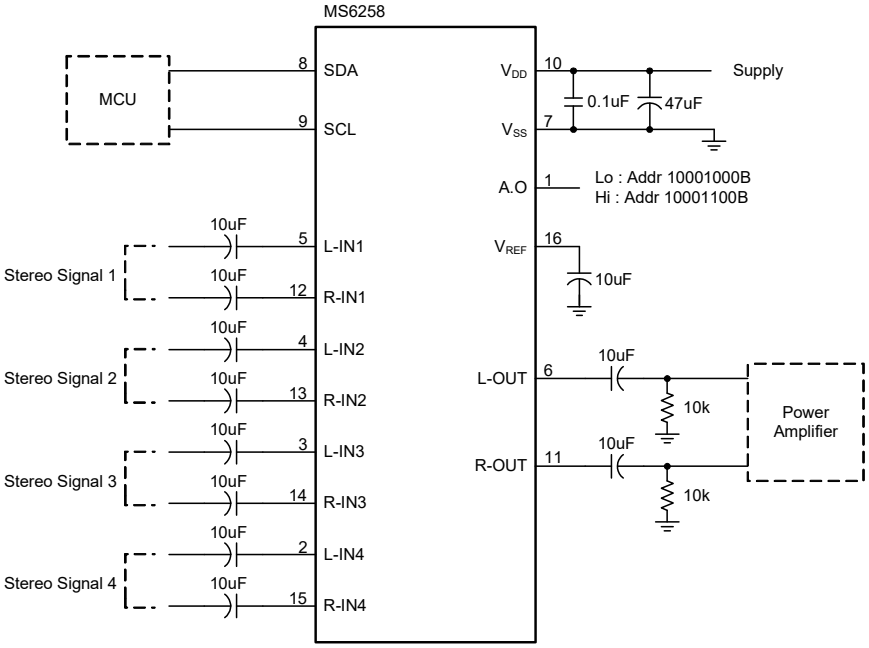
next, the volume changes from -14dB to +6dB. (Ax + Bx + Cx = 0dB + 0dB + 6dB)



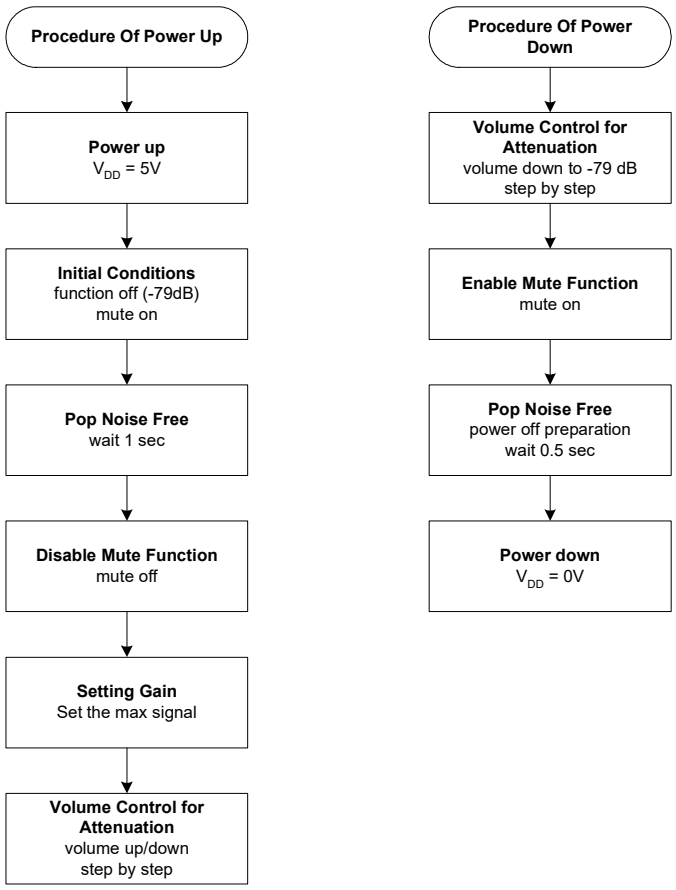
Note: We suggest the gain is set as the power is up. For example, set and fix the gain +10dB, the volume range will be controlled from +10dB to –69dB.

APPLICATION INFORMATION

Basic application example



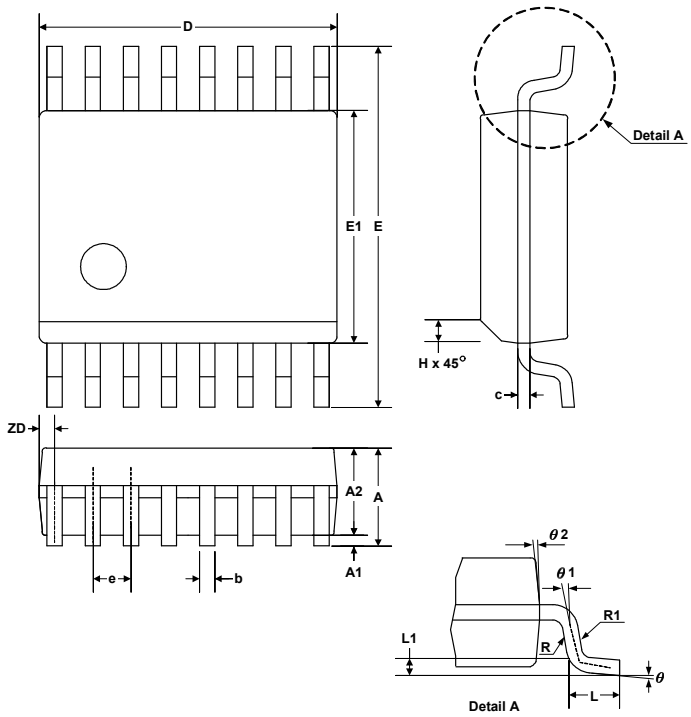
Basic application flowchart



1. The initial condition is –79dB, gain 0dB and mute on when power on.
2. In order to prevent pop noise when power on, please wait 1 sec to transmit I^2C command.

EXTERNAL DIMENSIONS

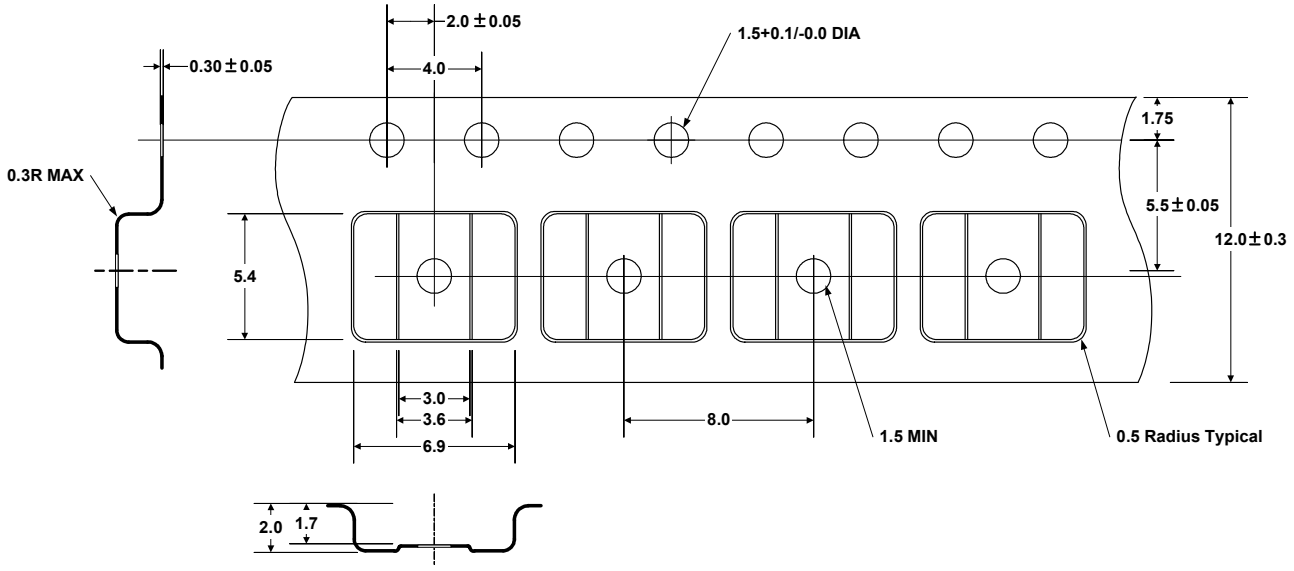
SSOP16



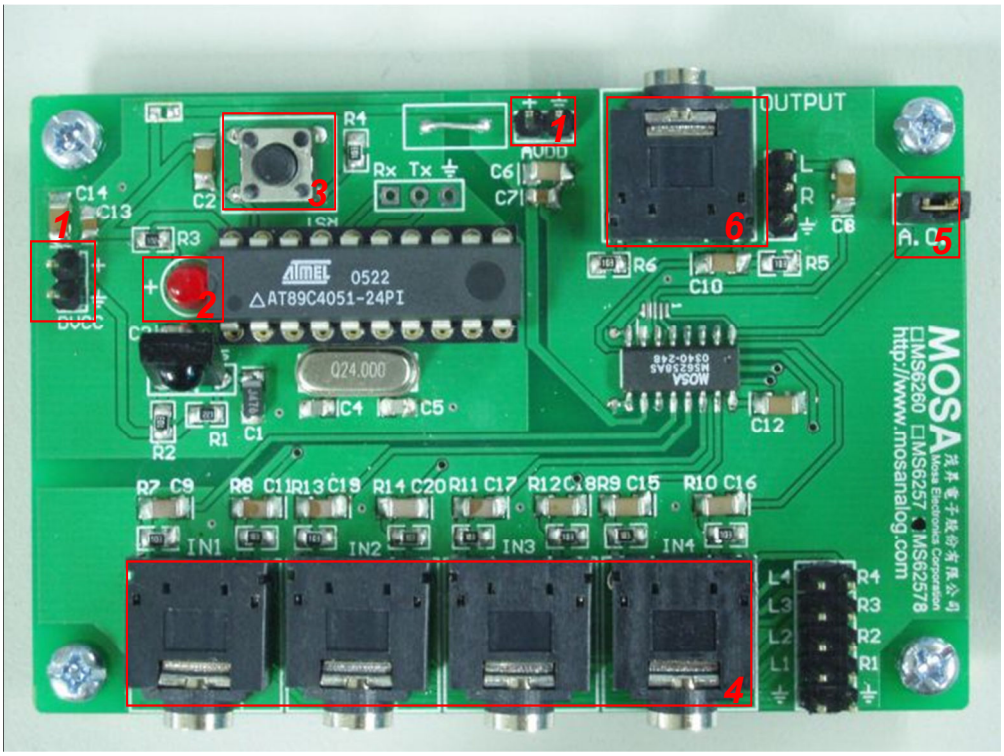
Symbol	Dimension in mm		Dimension in inch	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
A2		1.50		0.059
b	0.20	0.30	0.008	0.012
c	0.18	0.25	0.007	0.010
e	0.635 BASIC		0.025 BASIC	
D	4.80	5.00	0.189	0.197
E	5.79	6.20	0.228	0.244
E1	3.81	3.99	0.150	0.157
L	0.41	1.27	0.016	0.050
h	0.25	0.50	0.010	0.020
L1	0.254 BASIC		0.010 BASIC	
ZD	0.229 REF		0.009 REF	
R1	0.20	0.33	0.008	0.013
R	0.20		0.008	
θ	0°	8°	0°	8°
θ1	0°		0°	
θ2	5°	15°	5°	15°

TAPE AND REEL (Unit : mm)

SSOP16



DEMO BOARD



Function description

Label 1: Supply Voltage
The AVDD and DVDD should be the same supply voltage, the supply range is 2.7~6.5 VDC.

Label 2: LED Indicator
The LEDs indicate the chip status and IR received status. It keeps on a light state when the MS6257 is active. The other hand, keeps on a dark state when the MS6257 is power-off. It is red-dark blink once when the MCU has received the function code correctly.

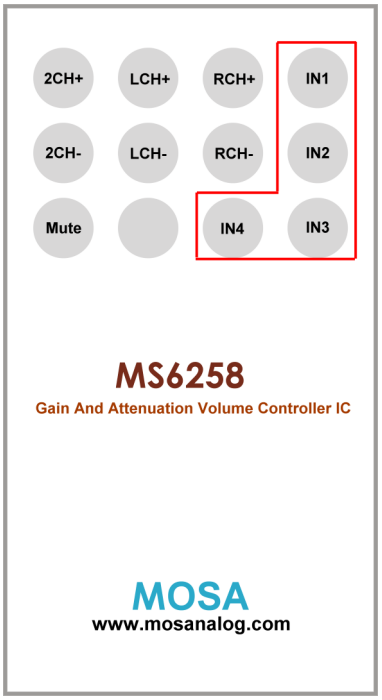
Label 3: Reset
All I/O pins are reset to default values. Volume 0dB and Mute on.

Label 4: Input section
Please input stereo audio signal, as music or sine wave.

Label 5: I2C Address option
As the jump is closed, the address code is 88H. As the jump is open, the address code is 8CH.

Label 6: Output section
Please connected to a post-power-amplifier, as stereo speaker.

IR Controller



2-CH+ : The volume-up switch for stereo channel
The volume increase by +1dB as the switch is pressed once, the maximum value is up to +15dB.
The default value is 0dB on initial status.
L-channel and R-channel are active synchronic.

2-CH- : The volume-down switch for stereo channel
The volume decrease by -1dB as the switch is pressed once, the minimum value is up to -79dB.
L-channel and R-channel are active synchronic.

LCH+ : The volume-up switch for left channel
The volume increase by +1dB as the switch is pressed once, the maximum value is up to +15dB.

LCH- : The volume-down switch for left channel
The volume decrease by -1dB as the switch is pressed once, the minimum value is up to -79dB.

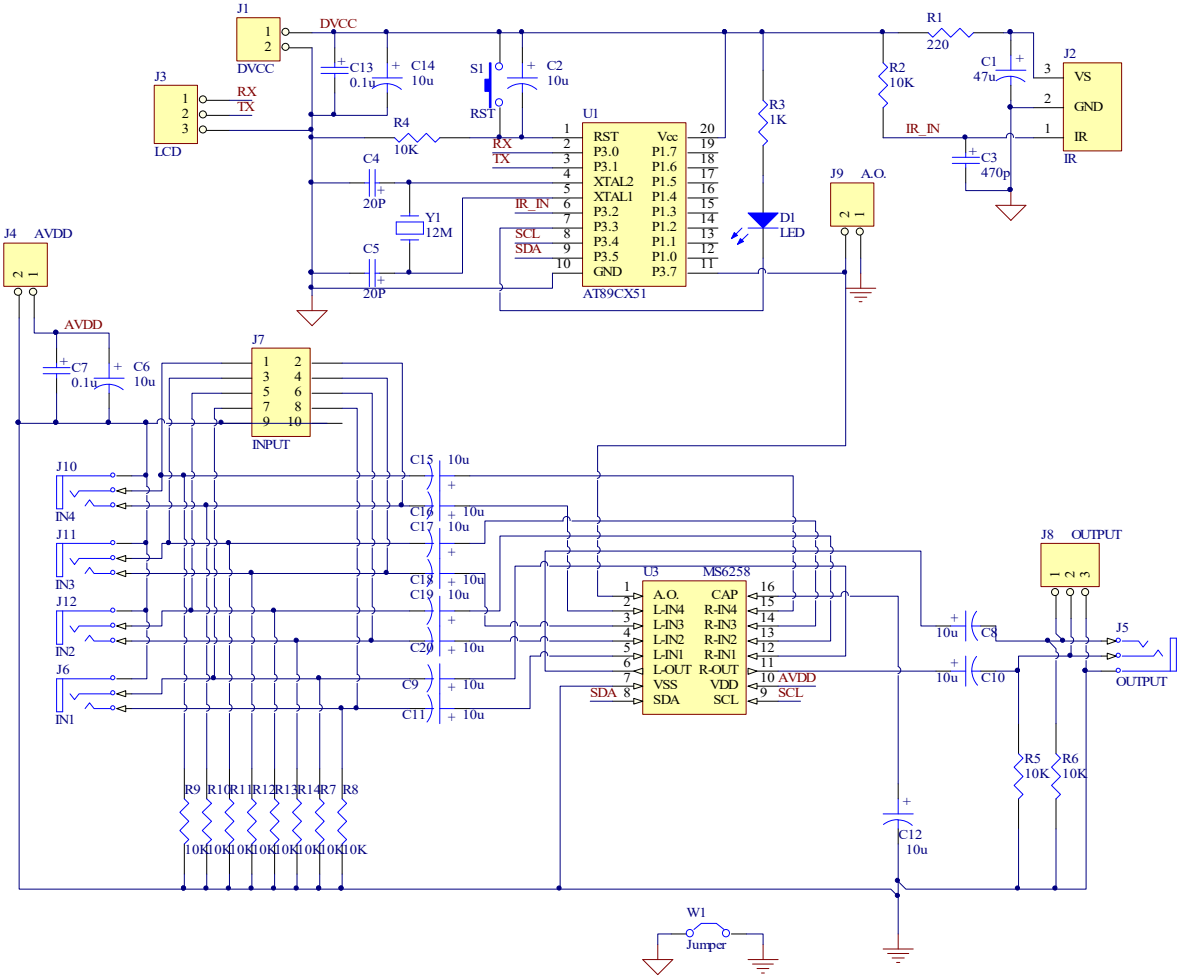
RCH+ : The volume-up switch for right channel
The volume increase by +1dB as the switch is pressed once, the maximum value is up to +15dB.

RCH- : The volume-down switch for right channel
The volume decrease by -1dB as the switch is pressed once, the minimum value is up to -79dB.

MUTE : Press the switch once to enter mute-on or mute-off.
The default status is mute-off on initial status.

IN1~IN4 : Stereo channel selection
There are four sets, stereo 1 to 4. The default channel is stereo 1 on initial status.

Circuit


J1
DVCC
J3
LCD
RX
TX
C13
0.1u
C14
10u
S1
RST
C2
10u
R4
10K
C4
20P
Y1
12M
C5
20P
U1
AT89CX51
RST
P3.0
P3.1
XTAL2
XTAL1
P3.2
P3.3
P3.4
P3.5
GND
Vcc
P1.7
P1.6
P1.5
P1.4
P1.3
P1.2
P1.1
P1.0
P3.7
IR_IN
SCL
SDA
R3
1K
D1
LED
R1
220
R2
10K
C1
47u
C3
470p
J2
VS
GND
IR
J9
A.O.
J4
AVDD
C7
0.1u
C6
10u
J7
INPUT
J10
IN4
J11
IN3
J12
IN2
J6
IN1
C15
C16
C17
C18
C19
C20
C9
C11
U3
MS6258
A.O.
L-IN4
L-IN3
L-IN2
L-IN1
L-OUT
VSS
SDA
CAP
R-IN4
R-IN3
R-IN2
R-IN1
R-OUT
VDD
SCL
J8
OUTPUT
J5
C8
C10
R5
10K
R6
10K
C12
10u
R9
R10
R11
R12
R13
R14
R7
R8
W1
Jumper