Low Cost 1 Stereo Input and 1 Stereo Output Volume, Tone, Balance, Loudness Function.

FEATURES

- Operation range : 2.7V~6.5V
- 2 independent speaker controls for balance
- Tone controls (treble and bass)
- Loudness and independent mute function
- Volume control in 1.25 dB/step
- I^2C interface
- Components less and good PSRR
- Housed in SSOP20 package
- Cost efficient.

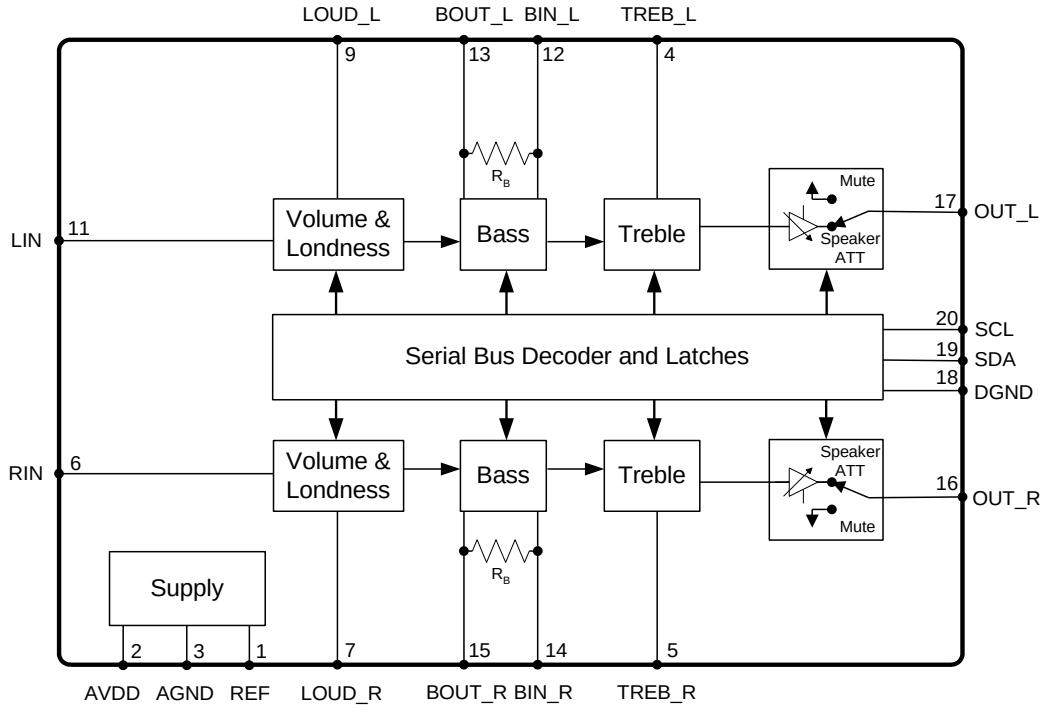
APPLICATIONS

- Portable audio device
- Car stereo audio
- Hi-Fi audio system

DESCRIPTION

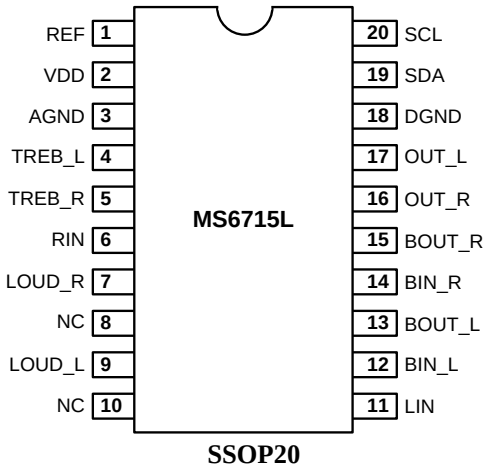
The MS6715L is a 1 stereo inputs/2-channel outputs digital control audio processor for the low voltage operation. Volume, tone (bass and treble), and balance (left/right) processor are incorporated into a single chip. The MS6715L also has the loudness function. These functions can be built a Hi-Fi audio system easily. All functions are programmable via the serial I^2C bus.
The default states of the chip as the power is on are: the volume is -78.75dB, all the speakers are mute and the gains of the bass and the treble are 0dB.

BLOCK DIAGRAM



PIN CONFIGURATION

Symbol	Pin	Description
REF	1	Analog Reference Voltage（1/2VDD）
VDD	2	Supply Input Voltage
AGND	3	Analog Ground
TREB_L	4	Left Channel Input for Treble Controller
TREB_R	5	Right Channel Input for Treble Controller
RIN	6	Right Channel Input
LOUD_R	7	Right Channel Loudness Input
NC	8	No Connected
LOUD_L	9	Left Channel Loudness Input
NC	10	No Connected
LIN	11	Left Channel Input
BIN_L	12	Left Bass Controller Input Channel
BOUT_L	13	Left Bass Controller Output Channel
BIN_R	14	Right Bass Controller Input Channel
BOUT_R	15	Right Bass Controller Output Channel
OUT_R	16	Right Speaker Output
OUT_L	17	Left Speaker Output
DGND	18	Digital Ground
SDA	19	I^2C Data Input
SCL	20	I^2C Clock Input



SSOP20

ORDERING INFORMATION

Package	Part number	Packaging Marking	Transport Media
20-Pin SSOP (lead free)	MS6715SSLTR	MS6715L	2.5k Units Tape and Reel
20-Pin SSOP (lead free)	MS6715SSLU	MS6715L	56 Units Tube

RoHS Compliance

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
V_{DD}	Supply Voltage	6.5	V
V_{ESD}	Electrostatic Handling	-3000 to 3000	V
T_{STG}	Storage Temperature Range	-65 to 150	℃
T_A	Operating Ambient Temperature Range	-40 to 85	℃
T_J	Maximum Junction Temperature	150	℃
T_S	Soldering Temperature, 10 seconds	260	℃
R_{THJA}	Thermal Resistance from Junction to Ambient in Free Air SSOP20	210	℃/W

OPERATING RATINGS

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply Voltage	2.7	-	6.5	V

5V ELECTRICAL CHARACTERISTICS

(Ta=25℃, All stages 0dB, f=1kHz, C_{REF} =22uF, refer to the application circuit; unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
I_Q	Quiescent Current	V_{IN}=0V	-	11.2	-	mA
PSRR	Power Supply Rejection Ratio	C_{REF} = 22uF, f = 100Hz	50	55	-	dB
Input						
R_{IN}	Input Resistance		35	50	70	kΩ
LOUD	Loudness	C_{Loud}=100nF, f =20Hz Volume=-40dB	18	20	-	dB
Volume control						
CR_{VOL}	Volume Control Range	Attenuation	-78.75	-	0	dB
RES_{VOL}	Volume Step Resolution		-	1.25	-	dB
ERR_{VOL}	Volume Setting Error	Av = 0 to -40dB	-1	0	1	dB
		Av = -40 to -60dB	-5	0	5	dB
Speaker Attenuators						
CR_{SPK}	Speaker Control Range	Attenuation	-37.5	-	0	dB
RES_{SPK}	Speaker Step Resolution		-	1.25	-	dB
ERR_{SPK}	Speaker Setting Error		-1	0	1	dB
MUTE	Output Mute Attenuation		-	-55	-50	dB
Bass Control						
CR_{BAS}	Bass Control Range	Boost/Cut	-14	-	14	dB
RES_{BAS}	Bass Step Resolution		-	2	-	dB
ERR_{BAS}	Speaker Setting Error	f =100Hz	-1	0	1	dB
R_B	Internal Feedback Resistance		34	44	58	kΩ
Treble Control						
CR_{BAS}	Treble Control Range	Boost/Cut	-14	-	14	dB
RES_{BAS}	Treble Step Resolution		-	2	-	dB
ERR_{BAS}	Treble Setting Error	f =20kHz	-1	0	1	dB
General						
VO_{MAX}	Maximum Output Voltage Swing	(THD+N)/S <0.3%	-	4.3	-	Vpp
THD+N	Total Harmonic Distortion Plus Noise	V_{OUT}=2Vpp	-	-65	-	dB
			-	0.056	-	%
S/N	Signal-to-Noise Ratio	V_{OUT}=4Vpp	-	85	-	dB
CS	Channel Separation Left/Right		80	85	-	dB
Bus Input						
V_{IH}	Bus High Input Level		2	-	-	V
V_{IL}	Bus Low Input Level		-	-	0.8	V

Notes:
Bass and Treble response see to curve. The center frequency and quality of the response behavior can be chosen by the external.

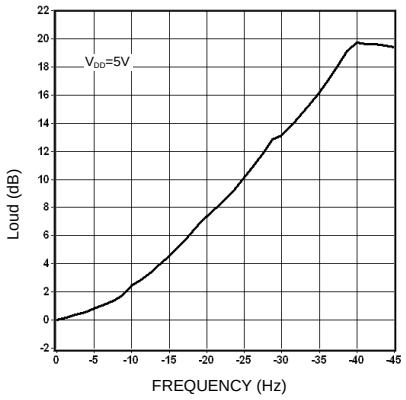
2.7V ELECTRICAL CHARACTERISTICS

(Ta=25℃, All stages 0dB, f=1kHz, C_{REF} =22uF, refer to the application circuit; unless otherwise specified)

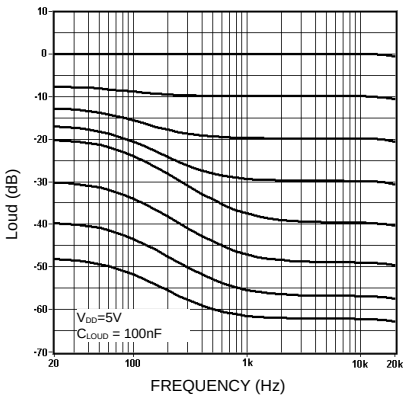
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
I_Q	Quiescent Current	V_{IN}=0V	-	8.7	-	mA
PSRR	Power Supply Rejection Ratio	C_{REF} = 22uF, f = 100Hz	48	53	-	dB
General						
VO_{MAX}	Maximum Output Voltage Swing	(THD+N)/S <0.3%	-	2.4	-	Vpp
THD+N	Total Harmonic Distortion Plus Noise	V_{OUT}=2Vpp	-	-48	-	dB
			-	0.4	-	%
S/N	Signal-to-Noise Ratio	V_{OUT}=2.4Vpp	80	85	-	dB
CS	Channel Separation Left/Right		80	85	-	dB

TYPICAL PERFORMANCE CHARACTERISTICS

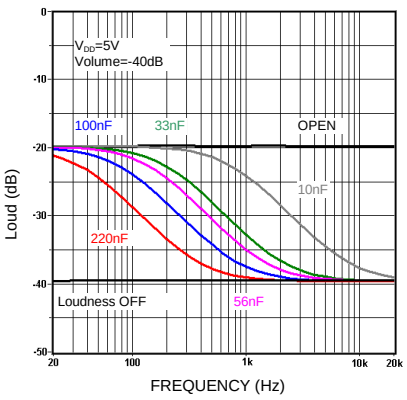
(Ta=25℃, All stages 0dB, f=1kHz, C_{REF} =22uF, refer to the application circuit; unless otherwise specified)



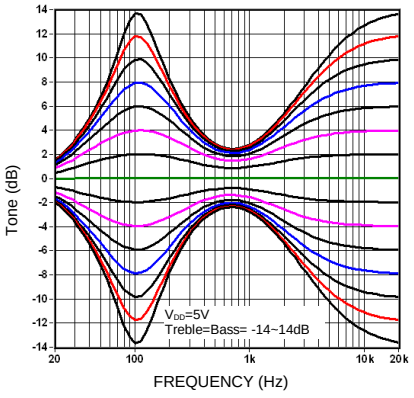
Loudness vs. Volume



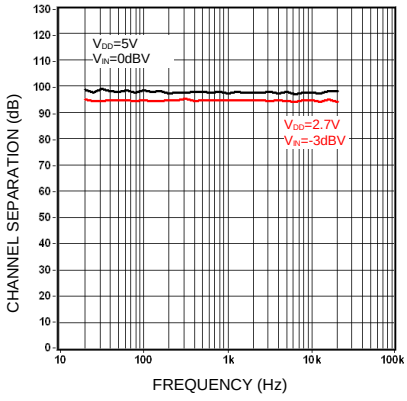
Loudness vs. Frequency vs. Volume



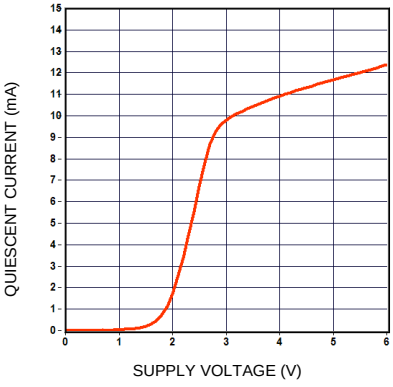
Loudness vs. External Capacitors



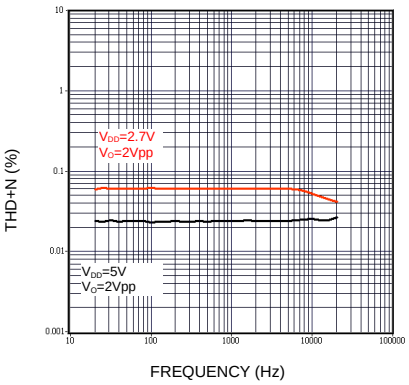
Typical Tone Response



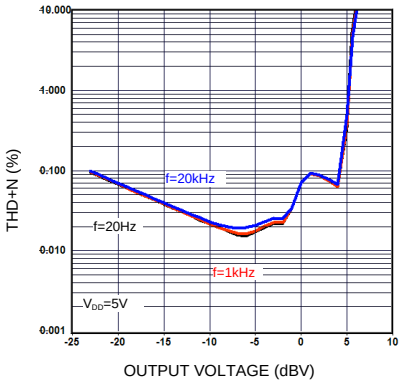
Channel Separation vs. Frequency



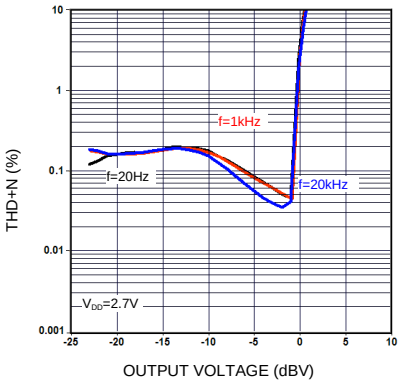
Quiescent Current vs. Supply Voltage



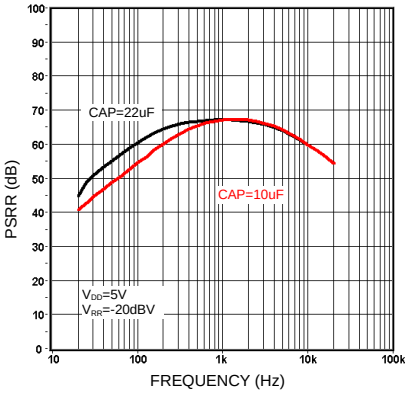
THD+N vs. Frequency



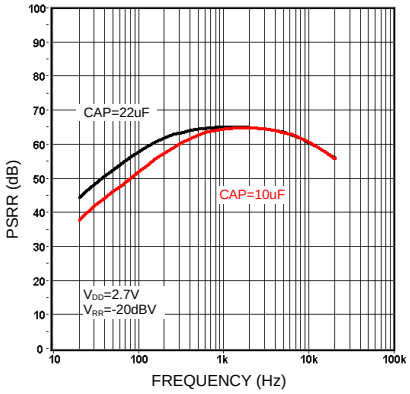
THD+N vs. Output Voltage



THD+N vs. Output Voltage



PSRR vs. Frequency

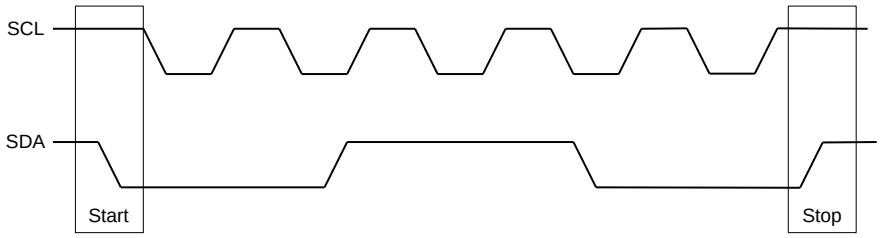


PSRR vs. Frequency

I²C BUS DESCRIPTION

Start and Stop Conditions

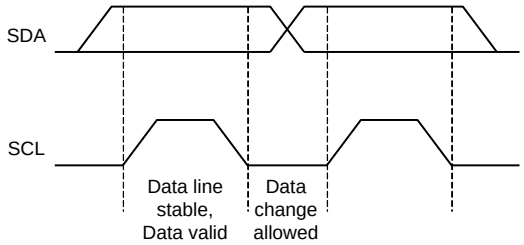
A start condition is activated when the SCL is set to HIGH and SDA shifts from HIGH to LOW state. The stop condition is activated when SCL is set to HIGH and SDA shifts from LOW to HIGH state. Please refer to the timing diagram below.



SCL : Serial Clock Line, SDA : Serial Data Line

Data Validity

A data on the SDA line is considered valid and stable only when the SCL signal is in HIGH state. The HIGH and LOW states of the SDA line can only change when the SCL signal is LOW. Please refer to the figure below.

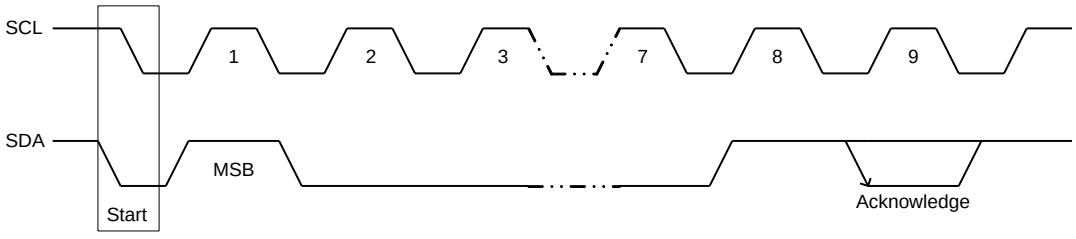


Byte Format

Every byte transmitted to the SDA line consists of 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transmitted first.

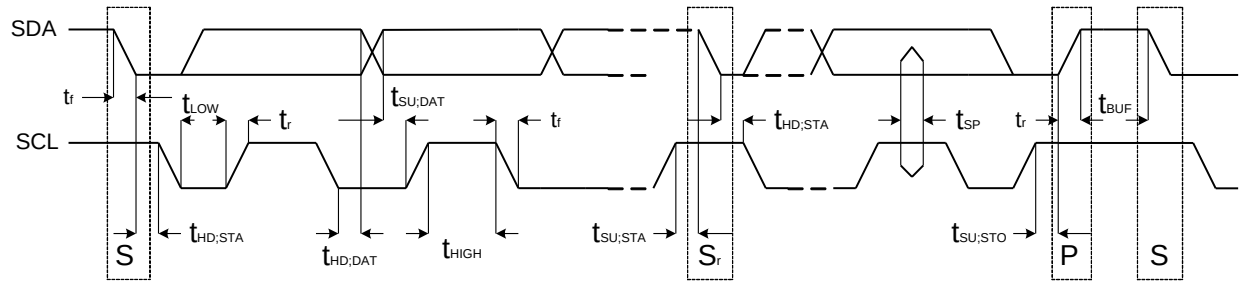
Acknowledge

During the Acknowledge clock pulse, the master (up) put a resistive HIGH level on the SDA line. The peripheral (audio processor) that acknowledges has to pull-down (LOW) the SDA line during the Acknowledge clock pulse so that the SDA line is in a stable LOW state during this clock pulse. Please refer to the diagram below.



The audio processor that has been addressed has to generate an Acknowledge after receiving each byte, otherwise, the SDA line will remain at the HIGH level during the ninth (9th) clock pulse. In this case, the master transmitter can generate the STOP information in order to abort the transfer.

Timing of SDA and SCL Bus Lines

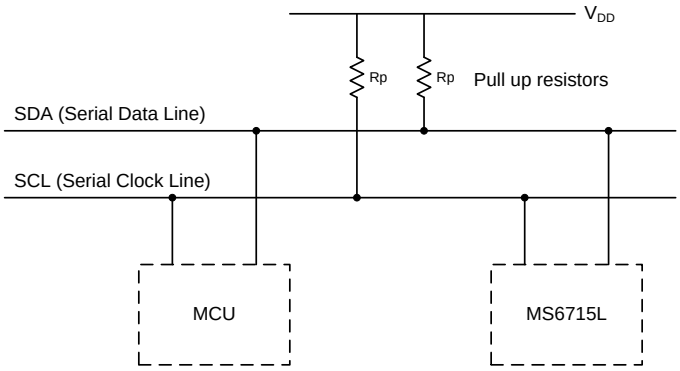


Standard Mode

Symbol	Parameter	Min	Max	Unit
f_{SCL}	SCL clock frequency	0	100	kHz
$t_{HD:STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated	4.0	-	us
t_{LOW}	LOW period of the SCL clock	4.7	-	us
t_{HIGH}	HIGH period of the SCL clock	4.0	-	us
$t_{SU:STA}$	Set-up time for a repeated START condition	4.7	-	us
$t_{HD:DAT}$	Data hold time: For I^2C-bus devices	0	3.45	us
$t_{SU:DAT}$	Data-set-up time	250	-	ns
t_r	Rise time of both SDA and SCL signals	-	1000	ns
t_f	Fall time of both SDA and SCL signals	-	300	ns
$t_{SU:STO}$	Set-up time for STOP condition	4.0	-	us
t_{BUF}	Bus free time between a STOP and START condition	4.7	-	us
C_b	Capacitive load for each bus line	-	400	pF
V_{nL}	Noise margin at the LOW level for each connected device (including hysteresis)	$0.1V_{DD}$	-	V
V_{nH}	Noise margin at the HIGH level for each connected device (including hysteresis)	$0.2V_{DD}$	-	V

BUS INTERFACE

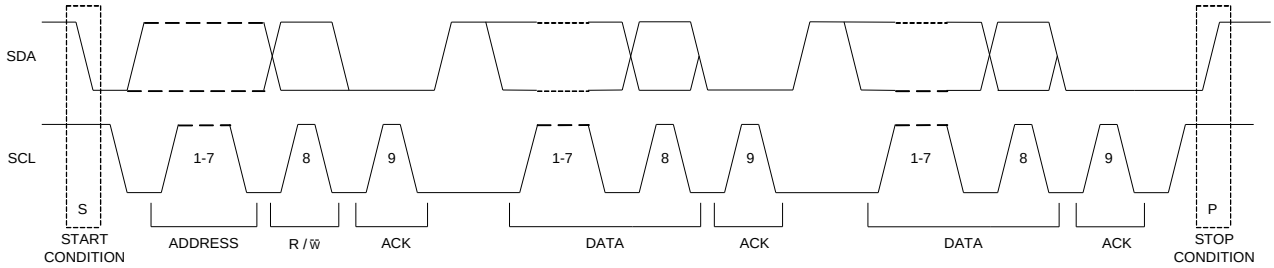
Data are transmitted to and from the MCU to the MS6715L via the SDA and SCL. The SDA and SCL make up the BUS interface. It should be noted that pull-up resistors must be connected to the positive supply voltage.



Interface Protocol

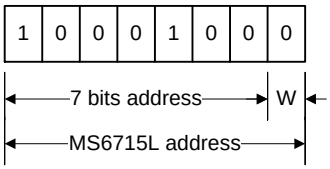
The format consists of the following

- A START condition
- A chip address byte including the MS6715L address. (7bits)
- The 8th bit of the byte must be "0".(write=0, read=1)
- MS6715L must always acknowledge the end of each transmitted byte.
- A data sequence (N-bytes + Acknowledge)
- A STOP condition



Address Code

The chip address of the MS6715L is 88H.



Data Bytes Description

The default states of the chip as the power is on are: the volume is -78.75dB, all the speakers are mute and the gains of the bass and the treble are 0dB.

MSB							LSB	Function
0	0	B2	B1	B0	A2	A1	A0	Volume Control
1	0	0	B1	B0	A2	A1	A0	Speaker ATT L
1	0	1	B1	B0	A2	A1	A0	Speaker ATT R
0	1	0	*	*	L	*	*	Loudness Control
0	1	1	0	C3	C2	C1	C0	Bass Control
0	1	1	1	C3	C2	C1	C0	Treble Control

Where Ax = 1.25dB steps; Bx = 10dB steps; Cx = 2dB steps; * = No effect

Volume

MSB							LSB	Function
0	**0**	**B2**	**B1**	**B0**	**A2**	**A1**	**A0**	**Volume 1.25 dB steps**
					0	0	0	0
					0	0	1	-1.25
					0	1	0	-2.5
					0	1	1	-3.75
					1	0	0	-5
					1	0	1	-6.25
					1	1	0	-7.5
					1	1	1	-8.75
0	**0**	**B2**	**B1**	**B0**	**A2**	**A1**	**A0**	**Volume 10dB steps**
		0	0	0				0
		0	0	1				-10
		0	1	0				-20
		0	1	1				-30
		1	0	0				-40
		1	0	1				-50
		1	1	0				-60
		1	1	1				-70

The default volume is –78.75dB.

Speaker Attenuator

MSB							LSB	Function（dB）
1	**0**	**0**	**B1**	**B0**	**A2**	**A1**	**A0**	**Speaker ATT L**
1	**0**	**1**	**B1**	**B0**	**A2**	**A1**	**A0**	**Speaker ATT R**
					0	0	0	0
					0	0	1	-1.25
					0	1	0	-2.5
					0	1	1	-3.75
					1	0	0	-5
					1	0	1	-6.25
					1	1	0	-7.5
					1	1	1	-8.75
			0	0				0
			0	1				-10
			1	0				-20
			1	1				-30
			1	1	1	1	1	Mute

The default state is mute.

Loudness

MSB							LSB	Function
0	**1**	**0**	**X**	**X**	**L**	**X**	**X**	**Loudness**
					0			Loudness ON
					1			Loudness OFF

The default state is loudness off.
X: don't care.

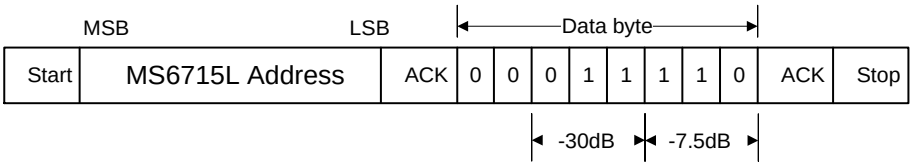
Bass and Treble

MSB							LSB	Function（dB）
0	**1**	**1**	**0**	**C3**	**C2**	**C1**	**C0**	**Bass**
0	**1**	**1**	**1**	**C3**	**C2**	**C1**	**C0**	**Treble**
				0	0	0	0	-14
				0	0	0	1	-12
				0	0	1	0	-10
				0	0	1	1	-8
				0	1	0	0	-6
				0	1	0	1	-4
				0	1	1	0	-2
				0	1	1	1	0
				1	1	1	1	0
				1	1	1	0	2
				1	1	0	1	4
				1	1	0	0	6
				1	0	1	1	8
				1	0	1	0	10
				1	0	0	1	12
				1	0	0	0	14

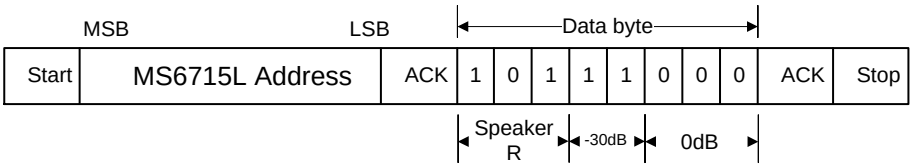
The default state is bass 0dB and treble 0dB.

Examples

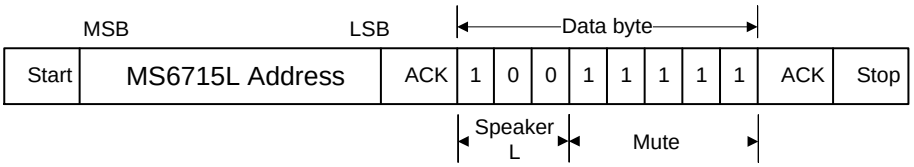
Set Volume at –37.5dB.



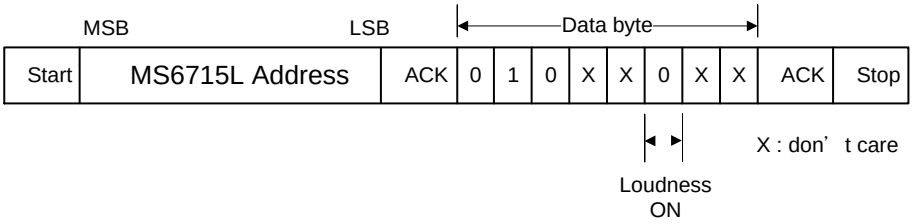
Set Speaker Right at -30dB.



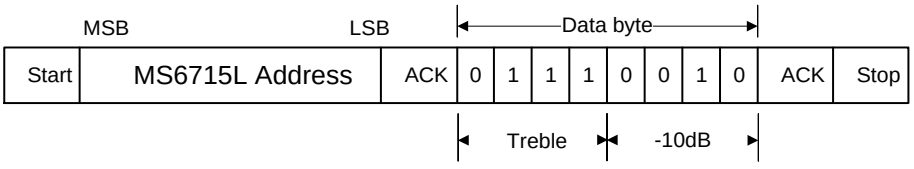
Set Speaker Left in mute-on.



Set Loudness in turn-on.

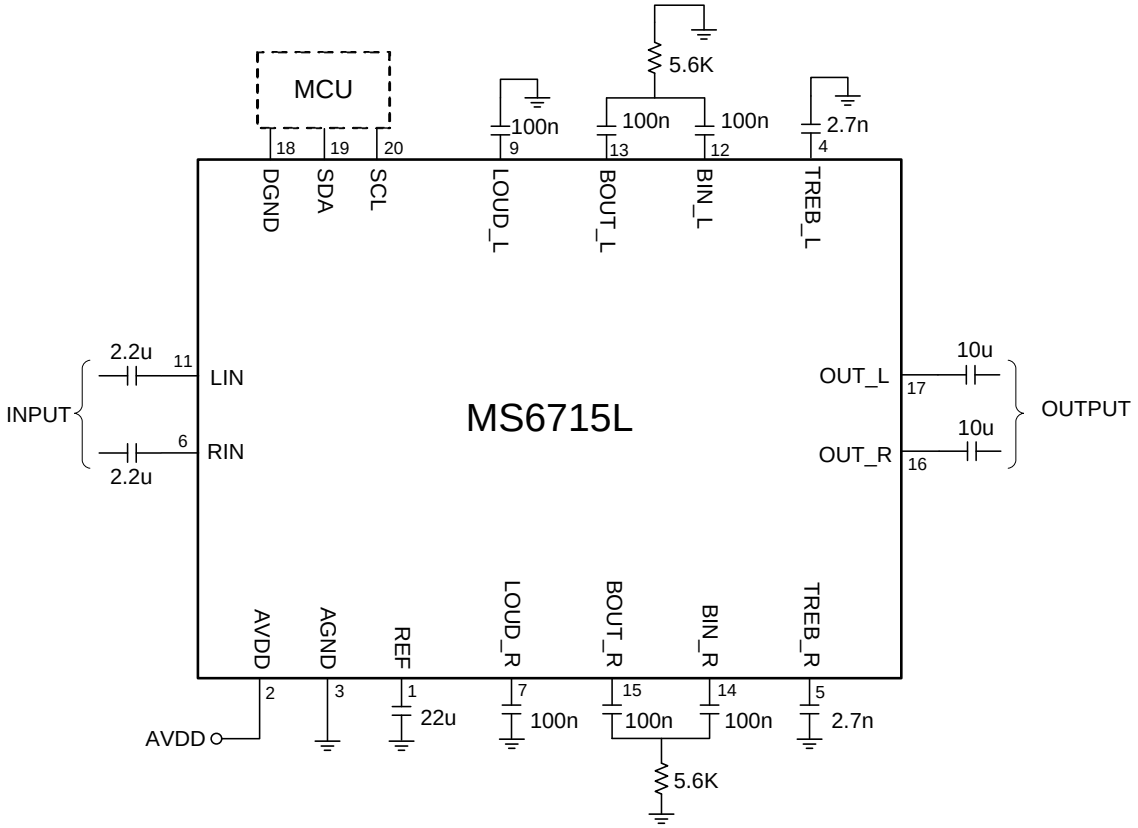


Set Treble at -10dB.



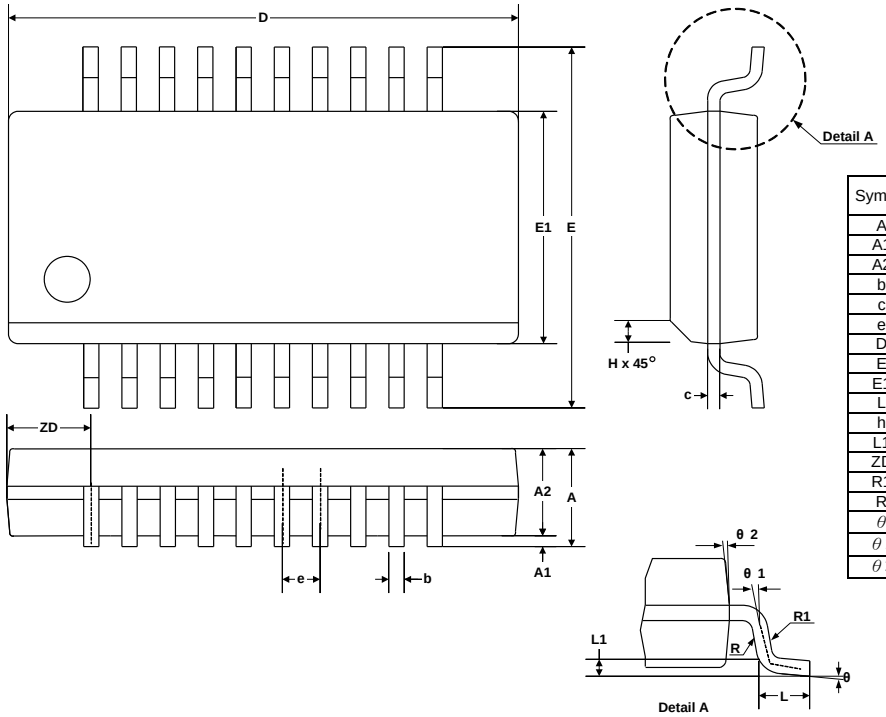
APPLICATION INFORMATION

Basic Application Example



EXTERNAL DIMENSIONS

SSOP20



Symbol	Dimension in mm		Dimension in inch	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
A2		1.50		0.059
b	0.20	0.30	0.008	0.012
c	0.18	0.25	0.007	0.010
e	0.635 BASIC		0.025 BASIC	
D	8.56	8.74	0.337	0.344
E	5.79	6.20	0.228	0.244
E1	3.81	3.99	0.150	0.157
L	0.41	1.27	0.016	0.050
h	0.25	0.50	0.010	0.020
L1	0.254 BASIC		0.010 BASIC	
ZD	1.4732 REF		0.058 REF	
R1	0.20	0.33	0.008	0.013
R	0.20		0.008	
θ	0^o	8^o	0^o	8^o
θ1	0^o		0^o	
θ2	5^o	15^o	5^o	15^o