DTMF Receiver

FEATURES

- Operating voltage : 4.5V~5.5V
- Low power consumption
- Internal gain setting amplifier
- Adjustable guard time
- Central office quality
- Power down mode
- Inhibit mode

APPLICATIONS

- Paging system
- Repeater systems
- Mobile radio
- Remote control

- Housed in SOP18(300mils), SSOP20(209mils) package

DESCRIPTION

The MS8870 is a complete DTMF receiver integrating both the bandsplit filter and digital decoder functions, fabricated in double poly technology and is pin and function compatible with MITEL 8870.
The filter section uses switched capacitor techniques for high and low group filters; the decoder uses digital counting techniques to detect and decode all 16 DTMF tone-pairs into a 4-bit code.
External component count is minimized by on chip provision of a differential input amplifier, clock oscillator and latched 3-state bus interface.

BLOCK DIAGRAM

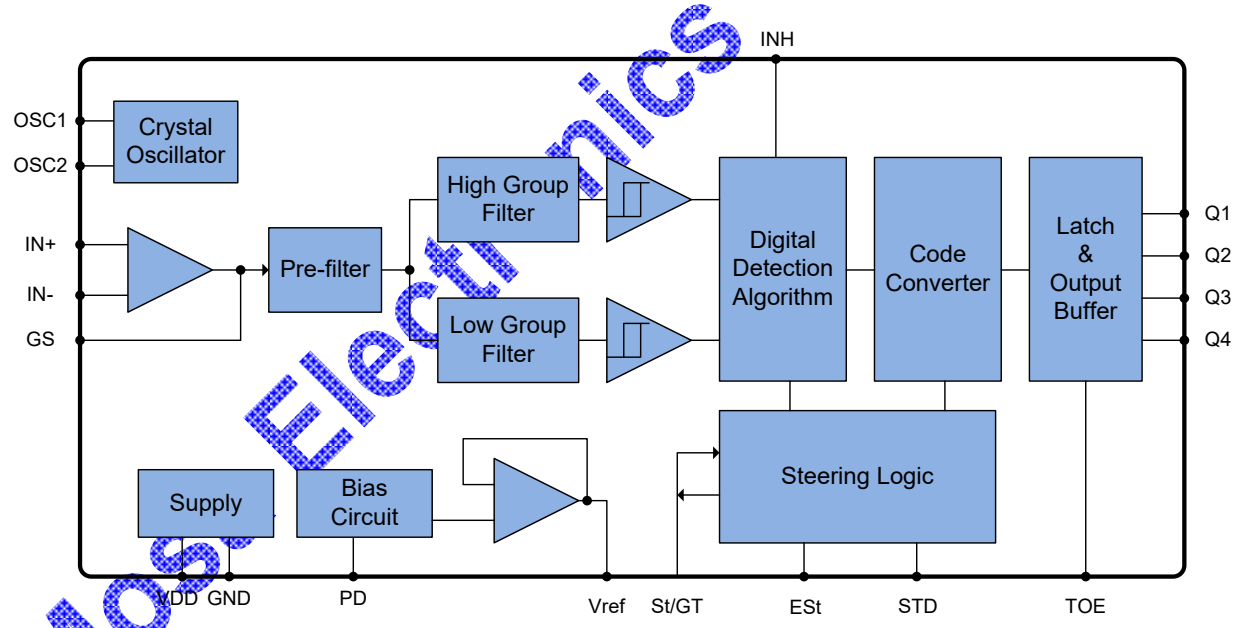
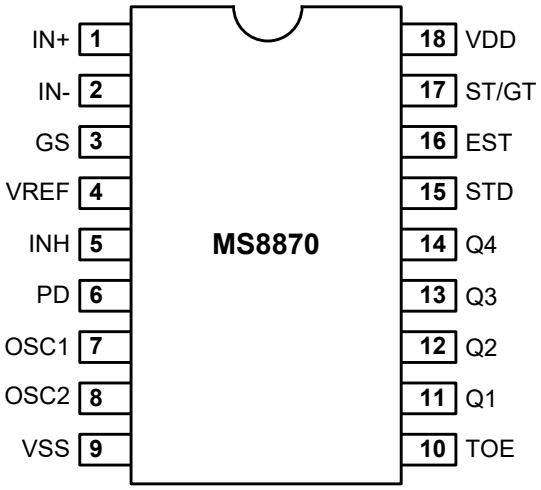


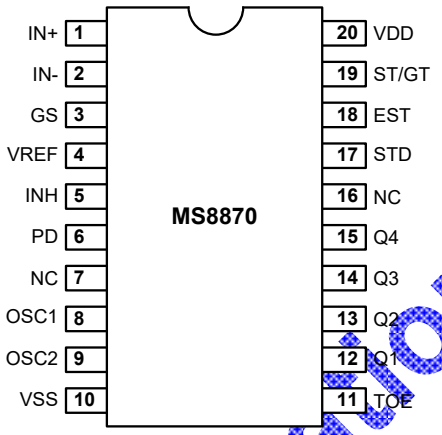
Figure 1. Functional Block Diagram

PIN CONFIGURATION

Symbol	Pin18	Pin20	I/O	Internal Connection	Description
IN+	1	1	I	Operational Amplifier	Operational amplifier non-inverting input.
IN-	2	2	I		Operational amplifier inverting input.
GS	3	3	O		**Gain Select.** Gives access to output of front end differential amplifier for connection of feedback resistor.
VREF	4	4	O	VREF	Reference Voltage output, nominally VDD/2.
INH	5	5	I	CMOS IN Pull-Low	**Inhibit.** Logic high inhibits the detection of tones representing characters A, B, C and D. This pin input is internally pulled down.
PD	6	6	I	CMOS IN Pull-Low	**Power Down.** Active high. Powers down the device and inhibits the oscillator. This pin input is internally pulled down.
NC	-	7	-		No Connected
OSC1	7	8	I	Oscillator	**Clock Input.**
OSC2	8	9	O		**Clock Output.** A 3.579545 MHz crystal connected between pins OSC1 and OSC2 completes the internal oscillator circuit.
V_{SS}	9	10	-	-	Ground
TOE	10	11	I	CMOS IN Pull-High	D0~D3 output enable, high active
Q1	11	12	O	CMOS OUT Tristate	Receiving data output terminals OE='H' : Output enable OE='L' : High impedance
Q2	12	13	O		
Q3	13	14	O		
Q4	14	15	O		
NC	-	16	-		No Connected
StD	15	17	O	CMOS OUT	**Delayed steering output.** Presents a logic high when a received tone-pair has been registered and the output latch updated; return to logic low when the voltage on St/GT falls below V_{TSt}.
ESt	16	18	O	CMOS OUT	**Early steering output.** Presents a logic high once the digital algorithm has detected a valid tone pair (signal condition). Any momentary loss of signal condition will cause ESt to return to a logic low.
St/GT	17	19	I/O	CMOS IN/ OUT	**Steering Input/Guard time Bidirectional.** A voltage greater than V_{TSt} detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than V_{TSt} frees the device to accept a new tone pair. The GT output acts to reset the external steering time-constant; its state is a function of ESt and the voltage on St.
V_{DD}	18	20	-	-	Positive power supply



SOP18(300mils)



SSOP20(209mils)

ORDERING INFORMATION

Package	Part number	Packaging Marking	Transport Media
18-Pin SOP (lead free)	MS8870GTR	MS8870G	2.5k Units Tape and Reel
18-Pin SOP (lead free)	MS8870GU	MS8870G	42 Units Tube
20-Pin SSOP (lead free)	MS8870SSGTR	MS8870G	2.5k Units Tape and Reel
20-Pin SSOP (lead free)	MS8870SSGU	MS8870G	66 Units Tube

RoHS Compliance

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply Voltage		6	V
V_I	Voltage on any pin	Vss-0.3	V_{DD}+0.3	V
I_I	Current at any pin		10	mA
T_A	Operating Ambient Temperature Range	-40	85	℃
T_{STG}	Storage Temperature Range	-65	150	℃
PD	Package power dissipation		1000	mW

DC ELECTRICAL CHARACTERISTICS (Ta = 25℃ V_{DD} = 5V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
V_{DD}	Operating Voltage		4.5	5	5.5	V
I_{DD}	Operating Current		-	2.0	5.5	mA
I_{STB}	Standby Current	PD = 5V	-	10	25	μA
INPUT						
V_{IL}	Low level input voltage				1.5	V
V_{IH}	High level input voltage		3.5			V
I_{IL}	Input leakage current	IN+ = IN- = Vss		0.1		μA
I_{IH}		IN+ = IN- = V_{DD}		0.1		μA
I_{SO}	Pull-up(source) current	V_{TOE}= 0V		7.5		μA
R_{IN}	Input Impedance(IN+ , IN-)			10		MΩ
V_{TSt}	Steering threshold voltage	V_{DD} = 5V	2.2	2.4	2.5	V
OUTPUT						
V_{OL}	Low level output voltage	No load			Vss+0.03	V
V_{OH}	High level output voltage	No load	V_{DD}-0.03			V
I_{OH}	Output high(Source) Current	V_{OUT} = 4.6V	0.4	0.8		mA
I_{OL}	Output Low(Sink) Current	V_{OUT} = 0.4V	1.0	2.5		mA
Vref	Vref output voltage	No load , V_{DD} = 5V	2.4	2.5	2.6	V
R_{OR}	Vref output resistance			1		kΩ

OPERATING CHARACTERISTICS GAIN SETTINGAMPLIFIER(Ta = 25℃ V_{DD} = 5V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{IN}	Input leakage current	Vss ≦ V_{IN} ≦ V_{DD}		100		nA
R_{IN}	Input resistance			10		MΩ
Vos	Input offset voltage			25		mV
PSRR	Power supply rejection	1KHz		60		dB
CMRR	Common mode rejection	-3.0V ≦ V_{IN} ≦ 3.0V		60		dB
A_{VOL}	DC open loop voltage gain			65		dB
Fc	Open loop unity gain bandwidth			1.5		MHz
Vo	Output voltage swing	R_L ≧ 100KΩ to Vss		4.5		Vpp
C_L	Maximum capacitive load (GS)			100		pF
R_L	Maximum resistive load (GS)			50		KΩ
V_{CM}	Common mode range	No Load		3.0		Vpp

AC ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V, T_A = 25℃, Fc = 3.579545 MHz, using test circuit shown in Figure 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SIGNAL COND						
	Valid input signal levels (each tone of composite signal)	Note.1,2,3,5,6,9	-31 21.8		+1 869	dBm mV_{RMS}
	Negative twist accept	Note.2,3,6,9		10		dB
	Positive twist accept	Note.2,3,6,9		10		dB
	Frequency deviation accept	Note.2,3,5,9	±1.5±2Hz			%
	Frequency deviation reject	Note.2,3,5,9	±3.5			%
	Third tone tolerance	Note.2,3,4,5,9,10		-16		dB
	Noise tolerance	Note.2,3,4,5,7,9,10		-12		dB
	Dial tone tolerance	Note.2,3,4,5,8,9,11		+22		dB
TIMING						
t_{DP}	Tone present detect time		5	11	14	ms
t_{DA}	Tone absent detect time		0.5	4	8.5	ms
t_{REC}	Tone duration accept	User adjustable			40	ms
$/t_{REC}$	Tone duration reject	User adjustable	20			ms
t_{ID}	Interdigit pause accept	User adjustable			40	ms
t_{DO}	Interdigit pause reject	User adjustable	20			ms
OUTPUT						
t_{PQ}	Propagation delay (St to Q)	TOE = V_{DD}		8	11	us
t_{PStD}	Propagation delay (St to StD)	TOE = V_{DD}		12		us
t_{QStD}	Output data set up (Q to StD)	TOE = V_{DD}		3.4		us
t_{PTE}	Propagation delay (TOE to Q ENABLE)	R_L = 10KΩ C_L = 50F		50		ns
t_{PTD}	Propagation delay (TOE to Q DISABLE)	R_L = 10KΩ C_L = 50F		300		ns
CLOCK						
Fc	Crystal / clock frequency		3.5759	3.5795	3.5831	MHz
t_{LHCL}	Clock input rise time	Ext. clock			110	ns
t_{HLCL}	Clock input fall time	Ext. clock			110	ns
DC_{DL}	Clock input duty cycle	Ext. clock	40	50	60	%
C_{LO}	Capacitive load (OSC2)				30	pF

NOTES

1. dBm = decibels above or below a reference power of 1 mW into a 600 ohm load.
2. Digit sequence consists of all 16 DTMF tones.
3. Tone duration = 40 ms, tone pause = 40 ms.
4. Signal condition consists of nominal DTMF frequencies.
5. Both tones in composite signal have an equal amplitude.
6. Tone pair is deviated by 1.5% ± 2Hz.
7. Bandwidth limited (3 KHz) Gaussian noise.
8. The precise dial tone frequencies are (350 Hz and 440 Hz) ± 2%.
9. For an error rate of better than 1 in 10,000.
10. Referenced to lowest level frequency component in DTMF signal.
11. Referenced to the minimum valid accept level.

Test circuit

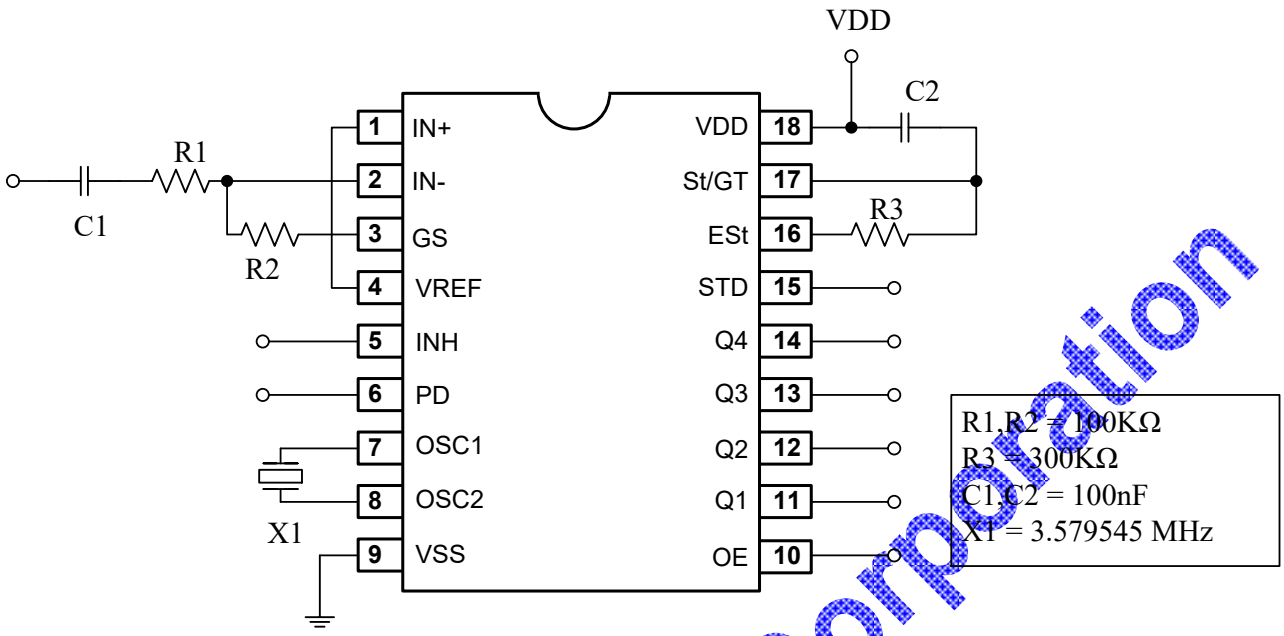


Figure 2. Single Ended Input Configuration

Timing Diagram

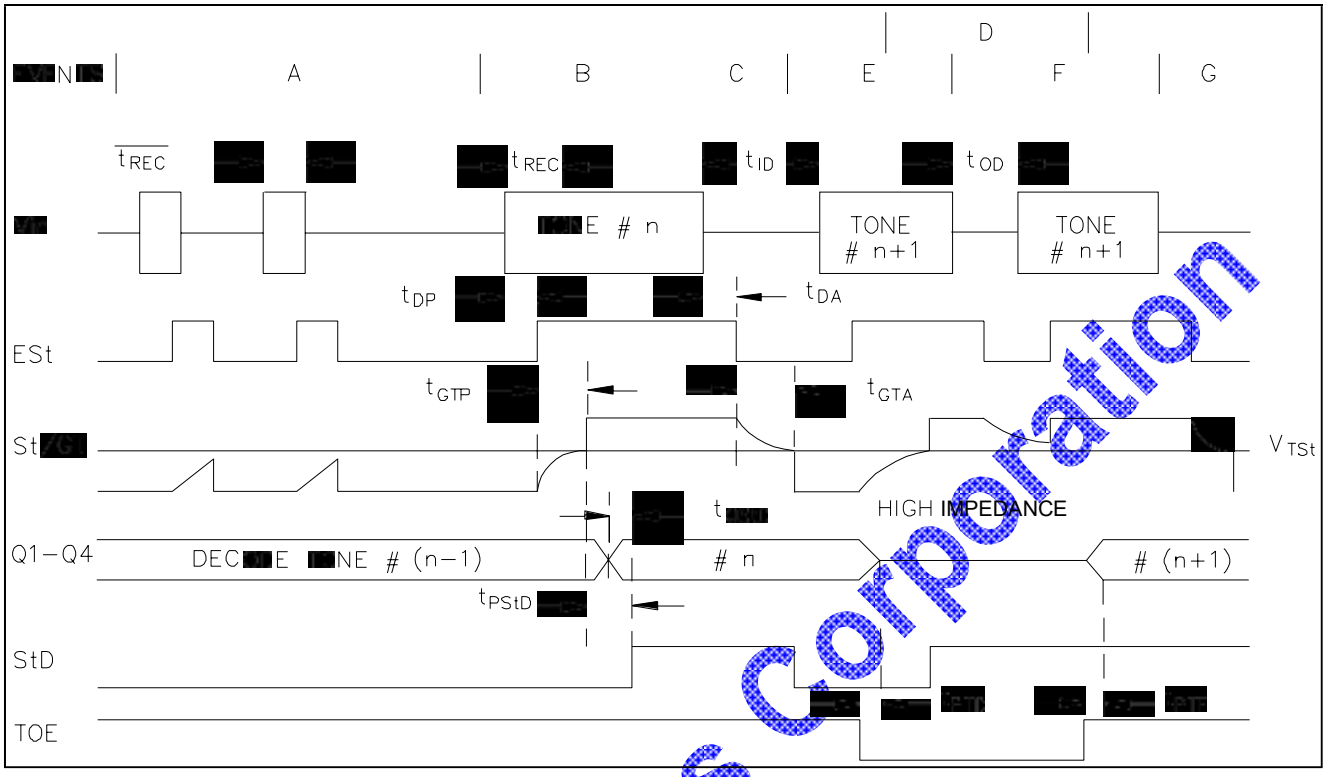


Figure 3. Timing Diagram

EXPLANATION OF EVENTS

A) Short tone bursts: detected. Tone duration is invalid.

B) Tone #n is detected. Tone duration is valid. Decoded to outputs.

C) End of Tone #n is detected and validated.

D) 3-State outputs disable (high impedance).

E) Tone #n + 1 is detected. Tone duration is valid. Decoded to outputs.

F) Tristate outputs are enabled. Acceptable drop out of Tone #n + 1 does not register at outputs.

G) End of Tone #n + 1 is detected and validated.

Functional Description

The MS8870 monolithic DTMF receiver offers small size, low power consumption and high performance. Its architecture consists of a bandsplit filter section, which separates the high and low group tones, followed by digital counting section which verifies the frequency and duration of the received tones before passing the corresponding code to the output bus.

Filter Section

Separation of the low-group and high-group tones is achieved by applying the DTMF signal to the inputs of two filters - a sixth order for the high group and an eighth order for the low group. The bandwidths of which correspond to the low and high group frequencies.

The filter section also incorporates notches at 350 and 440 Hz for exceptional dial tone rejection (see Fig. 4).

Each filter output is followed by a single order switched capacitor filter section which smooths the signals prior to limiting.

Limiting is performed by high-gain comparators which are provided with hysteresis to prevent detection of unwanted low-level signals.

The outputs of the comparators provide full rail logic swings at the frequencies of the incoming DTMF signals.

Decoder Section

The decoder uses digital counting techniques to determine the frequencies of limited tones and to verify that they correspond to standard DTMF frequencies.

A complex averaging algorithm protects against tone simulation by extraneous signals, such as voice, while providing tolerance to small frequency deviations and variations. This averaging algorithm has been developed to ensure an optimum combination of immunity to "talk-off" and tolerance to the presence of interfering signals ("third tones") and noise.

When the detector recognizes the simultaneous presence of two valid tone (referred to as "signal condition" in some industry specifications), it raises the "early steering" flag (ESt). Any subsequent loss of signal-condition will cause ESt to fall.

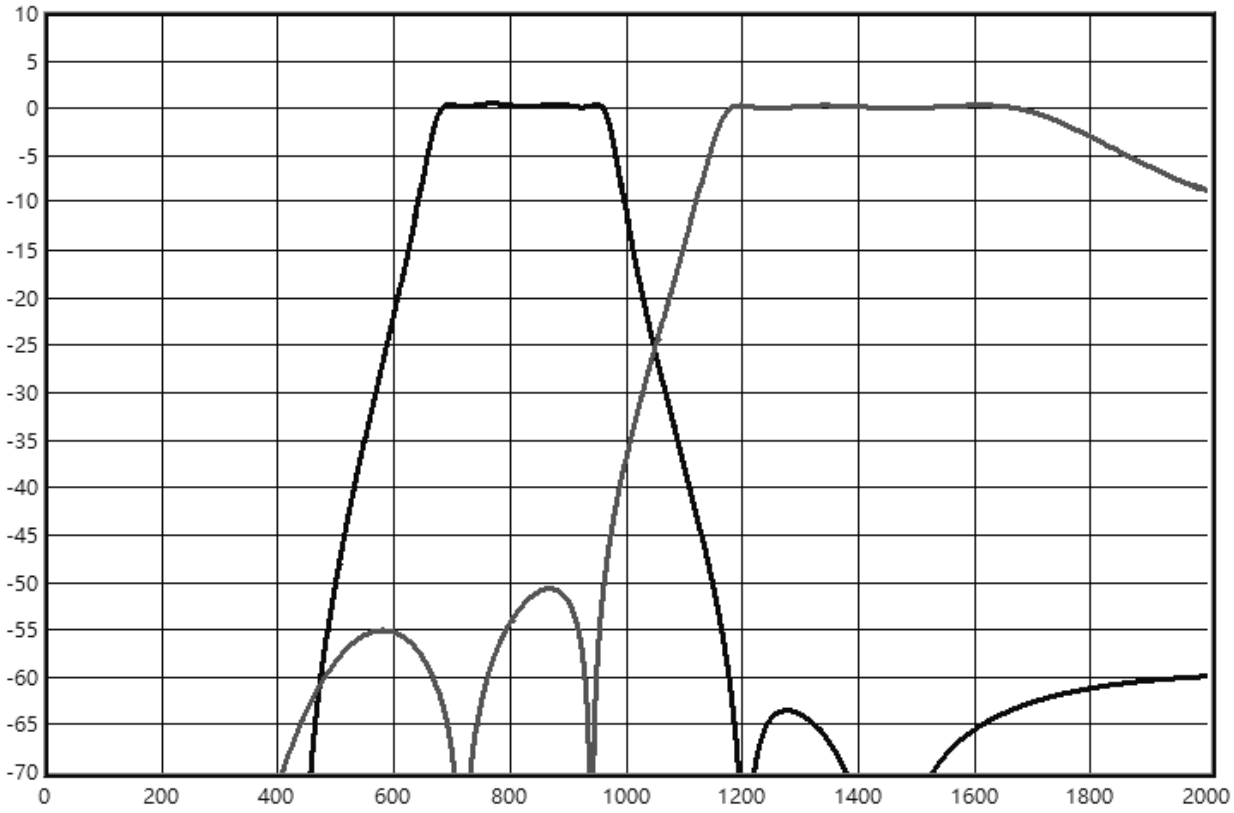


Figure 4 - Filter Response

FLOW	FHIGH	Digit	TOE	INH		Q4	Q3	Q2	Q1
697	1209	1	H	X		L	L	L	H
697	1366	2	H	X		L	L	H	L
697	1477	3	H	X		L	L	H	H
770	1209	4	H	X		L	H	L	L
770	1366	5	H	X		L	H	L	H
770	1477	6	H	X		L	H	H	L
852	1209	7	H	X		L	H	H	H
852	1366	8	H	X		H	L	L	L
852	1477	9	H	X		H	L	L	H
941	1209	0	H	X		H	L	H	L
941	1366	*	H	X		H	L	H	H
941	1477	#	H	X		H	H	L	L
697	1633	A	H	L		H	H	L	H
770	1633	B	H	L		H	H	H	L
852	1633	C	H	L		H	H	H	H
940	1633	D	H	L		L	L	L	L
697	1633	A	H	H		undetected, the output code will remain the same as the previous detected code			
770	1633	B	H	H					
852	1633	C	H	H					
940	1633	D	H	H					
		ANY	L			Z	Z	Z	Z

L = LOGIC LOW, H = LOGIC HIGH, Z = HIGH IMPEDANCE, X =DON'T CARE

Figure 5. Functional Decode Table

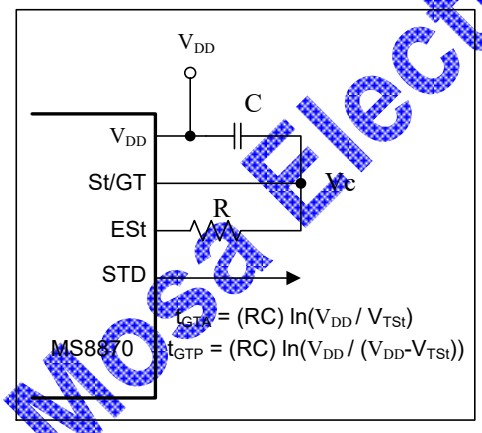


Figure 6. Basic Steering Circuit

Steering Circuit

Before registration of a decoded tone pair, the receiver checks for a valid signal duration (referred to as character recognition condition). This check is performed by an external RC time constant driven by ESt. A logic high on ESt causes Vc (see Fig. 6) to rise as the capacitor discharges.

Provided signal condition is maintained (ESt remains high) for the validation period (t_{GTP}), Vc reaches the threshold (V_{TSt}) of the steering logic to register the tone pair, latching latching its corresponding 4-bit code (see Fig. 5) into the output latch.

At this point the GT output is activated and drives Vc to VDD. GT continues to drive high as long as ESt remains high. Finally, after a short delay to allow the output latch to settle, the delayed steering output flag (StD) goes high, signaling that a received tone pair has been registered.

The contents of the output latch are made available on the 4-bit output bus by raising the three state control input (TOE) to a logic high. The steering circuit works in reverse to validate the inter digit pause between signals. Thus, as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions (drop out) too short to be considered a valid pause. This facility, together with the capability of selecting the steering time constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

Guard Time Adjustment

In many situations not requiring selection of tone duration and interdigital pause, the simple steering circuit shown in Fig. 6 is applicable. Component values are chosen according to the formula :

$$t_{REC} = t_{PD} + t_{GPT}$$
$$t_{ID} = t_{DA} + t_{GTA}$$

The value of t_{DP} is a device parameter (see table) and t_{REC} is the minimum signal duration to be recognized by the receiver. A value for C of 0.1uF is recommended for most applications, leaving R to be selected by the designer.

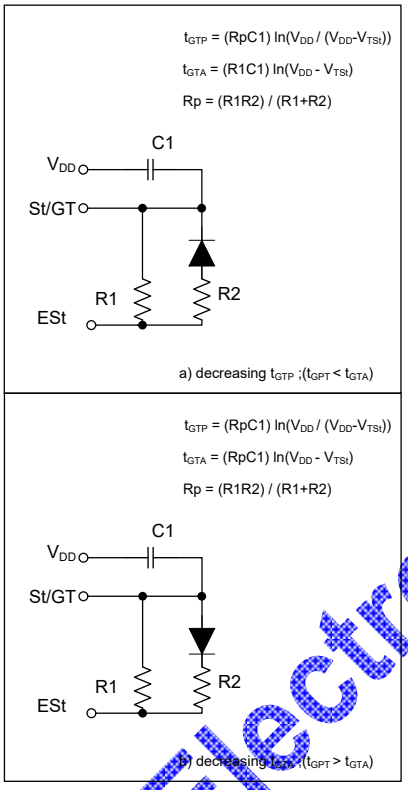


Figure 7. Guard Time Adjustment

Different steering arrangements may be used to select independently the guard times for tone present (t_{GTP}) and Ton absent (t_{GTA}). This may be necessary to meet system specifications which place both accept and reject limits on both tone duration and interdigital pause.

Guard time adjustment also allows the designer to tailor system parameters such as talk off and noise immunity. Increasing t_{REC} improves talk-off performance since it reduces the probability that tones simulated by speech will maintain signal condition long enough to be registered. Alternatively, a relatively short t_{REC} with noisy environments where fast acquisition time and immunity to tone drop-outs are required.

Design information for guard time adjustment is shown in Figure 7.

Differential Input Configuration

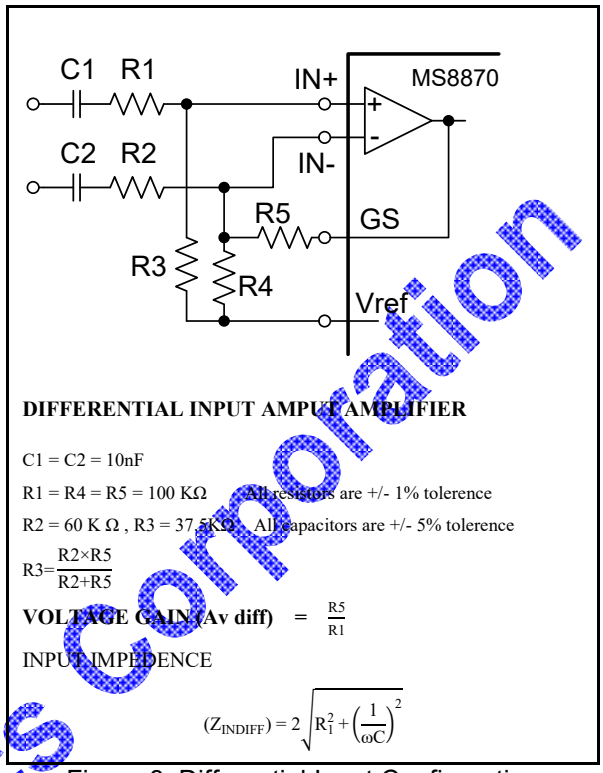


Figure 8. Differential Input Configuration

The input arrangement of the MS8870 provides a differential-input operational amplifier as well as a bias source (V_{Ref}) which is used to bias the inputs at mid-rail. Provision is made for connection of a feedback resistor to the op-amp output (GS) for adjustment of gain. In a single ended configuration, the input pins are connected as shown in Fig. 2 with the op-amp connected for unity gain and V_{Ref} biasing the input at $\frac{1}{2}V_{DD}$.

Fig. 8 shows the differential configuration, which permits the adjustment of gain with the feedback resistor R_5.

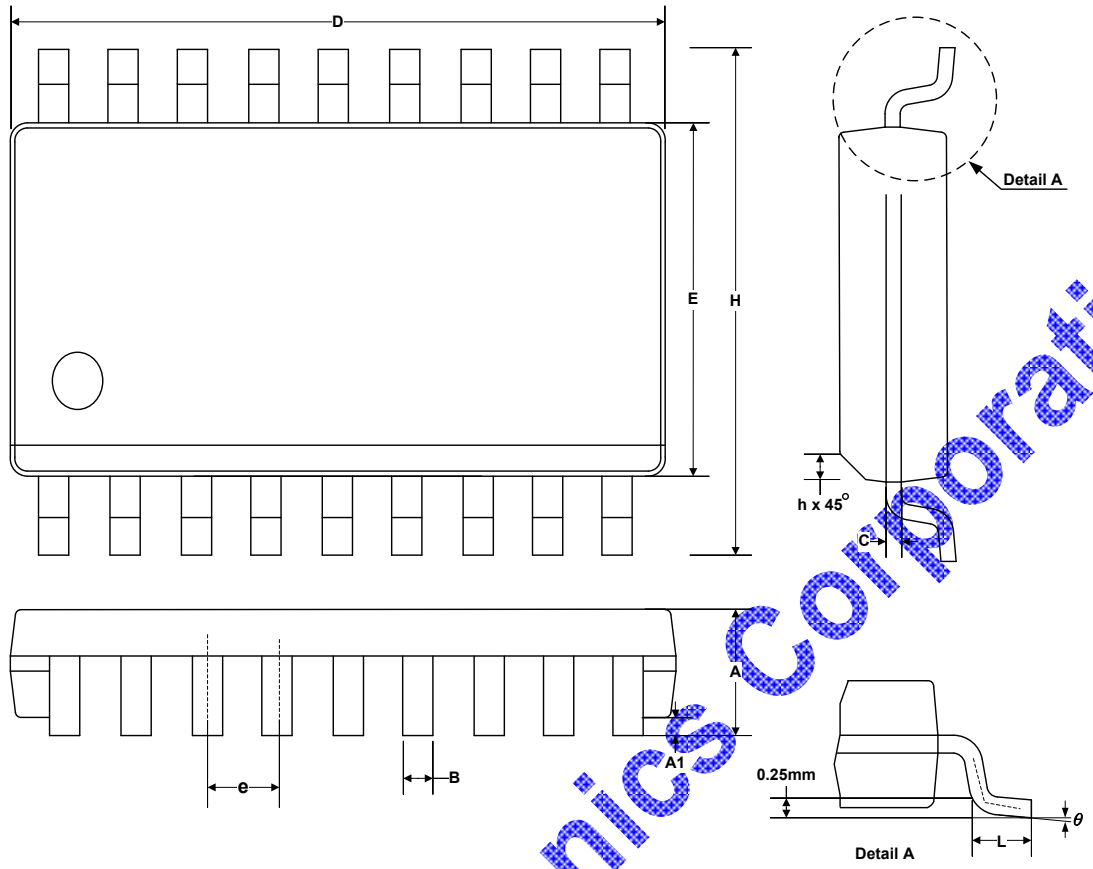
Power-down and Inhibit Mode

A logic high applied to pin 6 (PD) will power down the device to minimize the power consumption in a standby mode. It stops the oscillator and the functions of the filters.

Inhibit mode is enabled by a logic high input to the pin 5 (INH). It inhibits the detection of tones representing characters A, B, C, and D. The output code will remain the same as the previous detected code (see Figure 5).

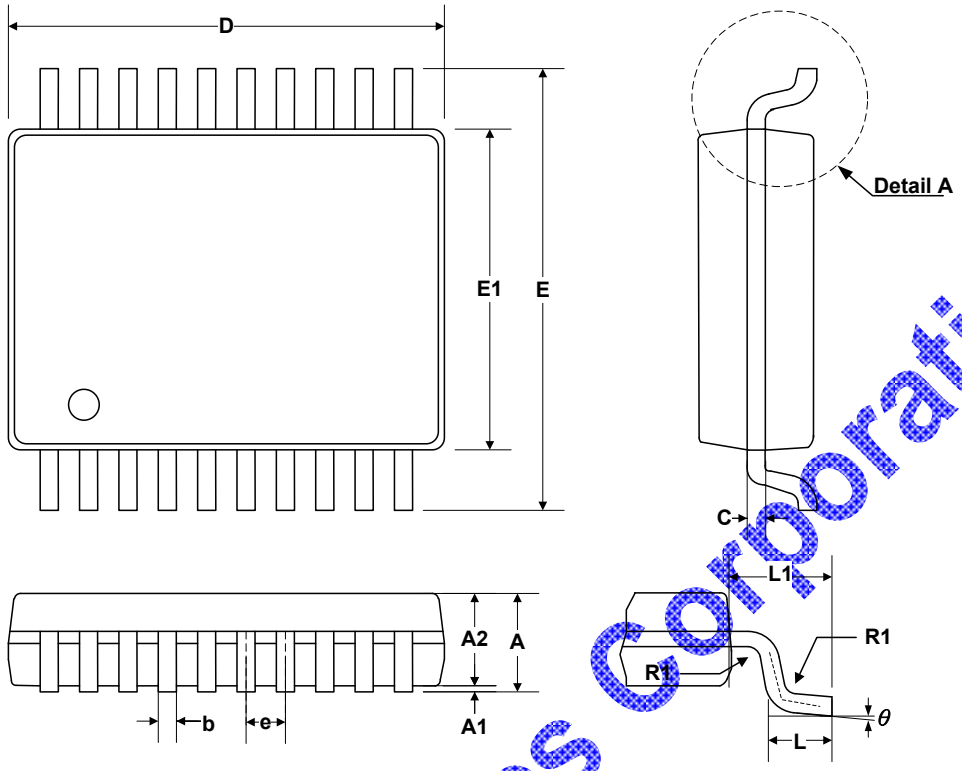
EXTERNAL DIMENSIONS

SOP18 (300mil)



Symbol	Dimension in mm			Dimension in inch		
	Min	NOM	Max	Min	NOM	Max
A	2.35		2.65	0.093		0.104
A1	0.10		0.30	0.004		0.012
B	0.33		0.51	0.013		0.020
C	0.23		0.32	0.009		0.013
E	1.27 BASIC			0.050 BASIC		
D	11.35		11.75	0.447		0.463
E	7.40		7.60	0.291		0.299
H	10.00		10.65	0.394		0.419
L	0.40		1.27	0.016		0.050
h	0.25	-	0.75	0.010	-	0.029
θ	0°	-	8°	0°	-	8°

SSOP20 (209mil)



Symbol	Dimension in mm			Dimension in inches		
	Min	Nom	Max	Min	Nom	Max
A	-	-	2	-	-	0.079
A1	0.05	-	-	0.002	-	-
A2	1.65	1.75	1.85	0.065	0.069	0.073
b	0.22	0.3	0.33	0.009	0.012	0.013
C	0.09	0.15	0.21	0.004	0.006	0.008
D	6.9	7.2	7.5	0.272	0.283	0.295
E	7.4	7.8	8.2	0.291	0.307	0.323
E1	5	5.3	5.6	0.197	0.209	0.220
e	0.650 BASIC			0.026 BASIC		
L	0.55	0.75	0.95	0.022	0.03	0.038
L1	1.25 REF.			0.049 REF.		
R1	0.09	-	-	0.004	-	-
θ	0	4	8	0	4	8